

AC784xx_DFP CKGEN

6.1.0

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Chapter 1

Class Index

1.1 Class List

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Chapter 2

File Index

2.1 File List

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Chapter 3

Class Documentation

3.1 Ckgen_ClkDistributeCfgType Struct Reference

Distribute clock configure structure.

```
#include <Ckgen_Hal.h>
```

Public Attributes

- uint8 [SysClkCfgCnt](#)
- uint16 [ClkDivCfgCnt](#)
- uint16 [ClkMuxCfgCnt](#)
- const [Ckgen_ClkDivCfgType](#) * [ClkDivCfgs](#)
- const [Ckgen_ClkMuxCfgType](#) * [ClkMuxCfgs](#)
- const [Ckgen_SysClkCfgType](#) * [SysClkCfgs](#)
- const [Ckgen_ClkoutCfgType](#) * [ClkoutCfg](#)

3.1.1 Detailed Description

Distribute clock configure structure.

Definition at line 174 of file Ckgen_Hal.h.

3.1.2 Member Data Documentation

3.1.2.1 ClkDivCfgCnt

```
uint16 Ckgen_ClkDistributeCfgType::ClkDivCfgCnt
```

Definition at line 177 of file Ckgen_Hal.h.

3.1.2.2 ClkDivCfgs

```
const Ckgen\_ClkDivCfgType* Ckgen_ClkDistributeCfgType::ClkDivCfgs
```

Definition at line 179 of file Ckgen_Hal.h.

3.1.2.3 ClkMuxCfgCnt

```
uint16 Ckgen_ClkDistributeCfgType::ClkMuxCfgCnt
```

Definition at line 178 of file Ckgen_Hal.h.

3.1.2.4 ClkMuxCfgs

```
const Ckgen\_ClkMuxCfgType* Ckgen_ClkDistributeCfgType::ClkMuxCfgs
```

Definition at line 180 of file Ckgen_Hal.h.

3.1.2.5 ClkoutCfg

```
const Ckgen\_ClkoutCfgType* Ckgen_ClkDistributeCfgType::ClkoutCfg
```

Definition at line 182 of file Ckgen_Hal.h.

3.1.2.6 SysClkCfgCnt

```
uint8 Ckgen_ClkDistributeCfgType::SysClkCfgCnt
```

Definition at line 176 of file Ckgen_Hal.h.

3.1.2.7 SysClkCfgs

```
const Ckgen\_SysClkCfgType* Ckgen_ClkDistributeCfgType::SysClkCfgs
```

Definition at line 181 of file Ckgen_Hal.h.

The documentation for this struct was generated from the following file:

- [Ckgen_Hal.h](#)

3.2 Ckgen_ClkDivCfgType Struct Reference

peripheral clock division configure structure.

```
#include <Ckgen_Hal.h>
```

Public Attributes

- uint8 [Div](#)
- Ckgen_ClkIdType [Clk](#)

3.2.1 Detailed Description

peripheral clock division configure structure.

Definition at line 74 of file Ckgen_Hal.h.

3.2.2 Member Data Documentation

3.2.2.1 Clk

```
Ckgen_ClkIdType Ckgen_ClkDivCfgType::Clk
```

to be configured clock id

Definition at line 77 of file Ckgen_Hal.h.

3.2.2.2 Div

```
uint8 Ckgen_ClkDivCfgType::Div
```

clock division

Definition at line 76 of file Ckgen_Hal.h.

The documentation for this struct was generated from the following file:

- [Ckgen_Hal.h](#)

3.3 Ckgen_ClkMuxCfgType Struct Reference

peripheral clock mux configure structure.

```
#include <Ckgen_Hal.h>
```

Public Attributes

- Ckgen_ClkIdType [Clk](#)
- Ckgen_ClkIdType [ClkSrc](#)

3.3.1 Detailed Description

peripheral clock mux configure structure.

Definition at line 65 of file Ckgen_Hal.h.

3.3.2 Member Data Documentation

3.3.2.1 Clk

```
Ckgen_ClkIdType Ckgen_ClkMuxCfgType::Clk
```

to be configured clock id

Definition at line 67 of file Ckgen_Hal.h.

3.3.2.2 ClkSrc

```
Ckgen_ClkIdType Ckgen_ClkMuxCfgType::ClkSrc
```

clock source id

Definition at line 68 of file Ckgen_Hal.h.

The documentation for this struct was generated from the following file:

- [Ckgen_Hal.h](#)

3.4 Ckgen_ClkoutCfgType Struct Reference

clkout clock configure structure.

```
#include <Ckgen_Hal.h>
```

Public Attributes

- boolean [Enable](#)
- Ckgen_ClkoutDivType [Div](#)
- Ckgen_ClkIdType [ClkSrc](#)

3.4.1 Detailed Description

clkout clock configure structure.

Definition at line 83 of file Ckgen_Hal.h.

3.4.2 Member Data Documentation

3.4.2.1 ClkSrc

```
Ckgen_ClkIdType Ckgen_ClkoutCfgType::ClkSrc
```

clock source id

Definition at line 87 of file Ckgen_Hal.h.

3.4.2.2 Div

```
Ckgen_ClkoutDivType Ckgen_ClkoutCfgType::Div
```

clock division

Definition at line 86 of file Ckgen_Hal.h.

3.4.2.3 Enable

```
boolean Ckgen_ClkoutCfgType::Enable
```

Enable or disable clock

Definition at line 85 of file Ckgen_Hal.h.

The documentation for this struct was generated from the following file:

- [Ckgen_Hal.h](#)

3.5 Ckgen_ClkSrcCfgType Struct Reference

clock source configure structure.

```
#include <Ckgen_Hal.h>
```

Public Attributes

- boolean [Enable](#)
- boolean [EnableInVLPS](#)
- uint8 [OutputDiv1](#)
- uint8 [OutputDiv2](#)
- Ckgen_ClkIdType [Clk](#)

3.5.1 Detailed Description

clock source configure structure.

Definition at line 138 of file Ckgen_Hal.h.

3.5.2 Member Data Documentation

3.5.2.1 Clk

```
Ckgen_ClkIdType Ckgen_ClkSrcCfgType::Clk
```

clock is VHSL or HSL

Definition at line 144 of file Ckgen_Hal.h.

3.5.2.2 Enable

```
boolean Ckgen_ClkSrcCfgType::Enable
```

Enable or disable clock

Definition at line 140 of file Ckgen_Hal.h.

3.5.2.3 EnableInVLPS

```
boolean Ckgen_ClkSrcCfgType::EnableInVLPS
```

[40][43]:HSL [42]:VHSL Enable or disable In VLPS

Definition at line 141 of file Ckgen_Hal.h.

3.5.2.4 OutputDiv1

```
uint8 Ckgen_ClkSrcCfgType::OutputDiv1
```

the value ranges 1 2 3 4 ... 63 64 [42][43]: 1 2 4 ...64

Definition at line 142 of file Ckgen_Hal.h.

3.5.2.5 OutputDiv2

```
uint8 Ckgen_ClkSrcCfgType::OutputDiv2
```

the value ranges 1 2 3 4 ... 63 64

Definition at line 143 of file Ckgen_Hal.h.

The documentation for this struct was generated from the following file:

- [Ckgen_Hal.h](#)

3.6 Ckgen_ClkTreeCfgType Struct Reference

Clock tree configure structure.

```
#include <Ckgen_Hal.h>
```

Public Attributes

- uint8 [ClkSrcCfgCnt](#)
- const [Ckgen_ClkSrcCfgType](#) * [ClkSrcCfgs](#)
- const [Ckgen_PllCfgType](#) * [pllCfg](#)
- const [Ckgen_XoscClkCfgType](#) * [XoscCfg](#)
- const [Ckgen_LPClkCfgType](#) * [LPCfg](#)
- const [Ckgen_ExternalClkFreqCfgType](#) * [ExtClkCfg](#)

3.6.1 Detailed Description

Clock tree configure structure.

Definition at line 188 of file Ckgen_Hal.h.

3.6.2 Member Data Documentation

3.6.2.1 ClkSrcCfgCnt

```
uint8 Ckgen_ClkTreeCfgType::ClkSrcCfgCnt
```

Definition at line 190 of file Ckgen_Hal.h.

3.6.2.2 ClkSrcCfgs

```
const Ckgen_ClkSrcCfgType* Ckgen_ClkTreeCfgType::ClkSrcCfgs
```

Definition at line 191 of file Ckgen_Hal.h.

3.6.2.3 ExtClkCfg

```
const Ckgen_ExternalClkFreqCfgType* Ckgen_ClkTreeCfgType::ExtClkCfg
```

Definition at line 195 of file Ckgen_Hal.h.

3.6.2.4 LPCfg

```
const Ckgen_LPClkCfgType* Ckgen_ClkTreeCfgType::LPCfg
```

Definition at line 194 of file Ckgen_Hal.h.

3.6.2.5 pllCfg

```
const Ckgen_PllCfgType* Ckgen_ClkTreeCfgType::pllCfg
```

Definition at line 192 of file Ckgen_Hal.h.

3.6.2.6 XoscCfg

```
const Ckgen_XoscClkCfgType* Ckgen_ClkTreeCfgType::XoscCfg
```

Definition at line 193 of file Ckgen_Hal.h.

The documentation for this struct was generated from the following file:

- [Ckgen_Hal.h](#)

3.7 Ckgen_ExternalClkFreqCfgType Struct Reference

external clock frequency configure structure.

```
#include <Ckgen_Hal.h>
```

Public Attributes

- uint32 [RtcClkInFreq](#)
- uint32 [PwmExtClk0Freq](#)
- uint32 [PwmExtClk1Freq](#)
- uint32 [PwmExtClk2Freq](#)

3.7.1 Detailed Description

external clock frequency configure structure.

Definition at line 104 of file Ckgen_Hal.h.

3.7.2 Member Data Documentation

3.7.2.1 PwmExtClk0Freq

```
uint32 Ckgen_ExternalClkFreqCfgType::PwmExtClk0Freq
```

Definition at line 107 of file Ckgen_Hal.h.

3.7.2.2 PwmExtClk1Freq

```
uint32 Ckgen_ExternalClkFreqCfgType::PwmExtClk1Freq
```

Definition at line 108 of file Ckgen_Hal.h.

3.7.2.3 PwmExtClk2Freq

```
uint32 Ckgen_ExternalClkFreqCfgType::PwmExtClk2Freq
```

Definition at line 109 of file Ckgen_Hal.h.

3.7.2.4 RtcClkInFreq

```
uint32 Ckgen_ExternalClkFreqCfgType::RtcClkInFreq
```

Definition at line 106 of file Ckgen_Hal.h.

The documentation for this struct was generated from the following file:

- [Ckgen_Hal.h](#)

3.8 Ckgen_LPClkCfgType Struct Reference

low power clock configure structure.

```
#include <Ckgen_Hal.h>
```

Public Attributes

- Ckgen_ClkIdType [LSIClkSrc](#)

3.8.1 Detailed Description

low power clock configure structure.

Definition at line 93 of file Ckgen_Hal.h.

3.8.2 Member Data Documentation

3.8.2.1 LSIClkSrc

```
Ckgen_ClkIdType Ckgen_LPClkCfgType::LSIClkSrc
```

clock source id

Definition at line 98 of file Ckgen_Hal.h.

The documentation for this struct was generated from the following file:

- [Ckgen_Hal.h](#)

3.9 Ckgen_PllCfgType Struct Reference

PLL clock configure structure.

```
#include <Ckgen_Hal.h>
```

Public Attributes

- boolean [Enable](#)
- boolean [EnableLD](#)
- uint8 [OutputDiv1](#)
- uint8 [OutputDiv2](#)
- Ckgen_ClkIdType [ClkSrc](#)
- Ckgen_PllLdDlySelType [DlySel](#)
- Ckgen_PllPreDivType [PreDiv](#)
- uint8 [FbkDiv](#)
- Ckgen_PllPosDivType [PosDiv](#)

3.9.1 Detailed Description

Pll clock configure structure.

Definition at line 115 of file Ckgen_Hal.h.

3.9.2 Member Data Documentation

3.9.2.1 ClkSrc

```
Ckgen_ClkIdType Ckgen_PllCfgType::ClkSrc
```

clock source is HSE or HSI

Definition at line 128 of file Ckgen_Hal.h.

3.9.2.2 DlySel

```
Ckgen_PllLdDlySelType Ckgen_PllCfgType::DlySel
```

Definition at line 129 of file Ckgen_Hal.h.

3.9.2.3 Enable

```
boolean Ckgen_PllCfgType::Enable
```

Enable or disable clock

Definition at line 117 of file Ckgen_Hal.h.

3.9.2.4 EnableLD

```
boolean Ckgen_PllCfgType::EnableLD
```

Enable or disable lock detect

Definition at line 118 of file Ckgen_Hal.h.

3.9.2.5 FbkDiv

```
uint8 Ckgen_PllCfgType::FbkDiv
```

the value ranges 5 6 7 ... 254 255

Definition at line 131 of file Ckgen_Hal.h.

3.9.2.6 OutputDiv1

```
uint8 Ckgen_PllCfgType::OutputDiv1
```

the value ranges 1 2 3 4 ... 63 64 [42][43]: 1 2 4 ...64

Definition at line 123 of file Ckgen_Hal.h.

3.9.2.7 OutputDiv2

```
uint8 Ckgen_PllCfgType::OutputDiv2
```

the value ranges 1 2 3 4 ... 63 64

Definition at line 124 of file Ckgen_Hal.h.

3.9.2.8 PosDiv

```
Ckgen_PllPosDivType Ckgen_PllCfgType::PosDiv
```

Definition at line 132 of file Ckgen_Hal.h.

3.9.2.9 PreDiv

`Ckgen_PllPreDivType Ckgen_PllCfgType::PreDiv`

Definition at line 130 of file `Ckgen_Hal.h`.

The documentation for this struct was generated from the following file:

- [Ckgen_Hal.h](#)

3.10 Ckgen_SysClkCfgType Struct Reference

system clock configure structure.

```
#include <Ckgen_Hal.h>
```

Public Attributes

- `Ckgen_SysClkModeType` [Mode](#)
- `Ckgen_ClkIdType` [ClkSrc](#)
- `uint8` [SysDiv](#)
- `uint8` [BusDiv](#)

3.10.1 Detailed Description

system clock configure structure.

Definition at line 163 of file `Ckgen_Hal.h`.

3.10.2 Member Data Documentation

3.10.2.1 BusDiv

`uint8 Ckgen_SysClkCfgType::BusDiv`

the value ranges 1 2 3 4 ... 15 16

Definition at line 168 of file `Ckgen_Hal.h`.

3.10.2.2 ClkSrc

`Ckgen_ClkIdType Ckgen_SysClkCfgType::ClkSrc`

the value ranges RUN: VHSE, HSE, HSI, PLL; VLPR: HSI

Definition at line 166 of file `Ckgen_Hal.h`.

3.10.2.3 Mode

```
Ckgen_SysClkModeType Ckgen_SysClkCfgType::Mode
```

the value ranges RUN or VLPR mode

Definition at line 165 of file Ckgen_Hal.h.

3.10.2.4 SysDiv

```
uint8 Ckgen_SysClkCfgType::SysDiv
```

the value ranges 1 2 3 4 ... 15 16

Definition at line 167 of file Ckgen_Hal.h.

The documentation for this struct was generated from the following file:

- [Ckgen_Hal.h](#)

3.11 Ckgen_XoscClkCfgType Struct Reference

Xosc clock configure structure.

```
#include <Ckgen_Hal.h>
```

Public Attributes

- boolean [Enable](#)
- boolean [EnableBypass](#)
- boolean [EnableMonitor](#)
- uint8 [OutputDiv1](#)
- uint8 [OutputDiv2](#)
- uint32 [Freq](#)

3.11.1 Detailed Description

Xosc clock configure structure.

Definition at line 150 of file Ckgen_Hal.h.

3.11.2 Member Data Documentation

3.11.2.1 Enable

```
boolean Ckgen_XoscClkCfgType::Enable
```

Enable or disable HSE

Definition at line 152 of file Ckgen_Hal.h.

3.11.2.2 EnableBypass

```
boolean Ckgen_XoscClkCfgType::EnableBypass
```

true:use OSC_IN false:OSC_IN ???

Definition at line 153 of file Ckgen_Hal.h.

3.11.2.3 EnableMonitor

```
boolean Ckgen_XoscClkCfgType::EnableMonitor
```

HSE disable and Enable EnableMonitor it causes the system reboot

Definition at line 154 of file Ckgen_Hal.h.

3.11.2.4 Freq

```
uint32 Ckgen_XoscClkCfgType::Freq
```

clock frequency

Definition at line 157 of file Ckgen_Hal.h.

3.11.2.5 OutputDiv1

```
uint8 Ckgen_XoscClkCfgType::OutputDiv1
```

[40] the value ranges 1 2 3 4 ... 63 64 [42][43]: 1 2 4 ...64

Definition at line 155 of file Ckgen_Hal.h.

3.11.2.6 OutputDiv2

```
uint8 Ckgen_XoscClkCfgType::OutputDiv2
```

the value ranges 1 2 3 4 ... 63 64

Definition at line 156 of file Ckgen_Hal.h.

The documentation for this struct was generated from the following file:

- [Ckgen_Hal.h](#)

Chapter 4

File Documentation

4.1 AC784xx_API_Reference_Manual_CKGEN.pdf File Reference

4.2 AC784xx_Ckgen_Reg.c File Reference

ckgen hal source file.

```
#include "AC784xx_Ckgen_Reg.h"
```

Functions

- void [Ckgen_Reg_SetCanClkDiv](#) (Ckgen_ClkIdType Clk, uint8 Div)
Set can clock division.
- uint8 [Ckgen_Reg_GetCanClkDiv](#) (Ckgen_ClkIdType Clk)
Get can clock division.
- void [Ckgen_Reg_SetSPLLClkMux](#) (Ckgen_ClkIdType ClkSrc)
Set spll clock mux.
- Ckgen_ClkIdType [Ckgen_Reg_GetSPLLClkMux](#) (void)
get spll mux
- void [Ckgen_Reg_SetClkoutClkMux](#) (Ckgen_ClkIdType ClkSrc)
Set clkout clock mux.
- Ckgen_ClkIdType [Ckgen_Reg_GetClkoutClkMux](#) (void)
get clockout mux
- void [Ckgen_Reg_SetCommPeriphClkMux](#) (Ckgen_ClkIdType Clk, Ckgen_ClkIdType ClkSrc)
Set common peripheral clkout clock mux.
- void [Ckgen_Reg_SetPwmClkMux](#) (Ckgen_ClkIdType Clk, Ckgen_ClkIdType ClkSrc)
Set pwm clock mux.
- void [Ckgen_Reg_SetCanClkMux](#) (Ckgen_ClkIdType Clk, Ckgen_ClkIdType ClkSrc)
Set can clock mux.
- Ckgen_ClkIdType [Ckgen_Reg_GetCommPeriphClkMux](#) (Ckgen_ClkIdType Clk)
get common peripheral clock mux
- Ckgen_ClkIdType [Ckgen_Reg_GetPwmClkMux](#) (Ckgen_ClkIdType Clk)
Get pwm clock mux.
- Ckgen_ClkIdType [Ckgen_Reg_GetCanClkMux](#) (Ckgen_ClkIdType Clk)
Get can clock mux.

4.2.1 Detailed Description

ckgen hal source file.

4.2.2 Function Documentation

4.2.2.1 Ckgen_Reg_GetCanClkDiv()

```
uint8 Ckgen_Reg_GetCanClkDiv (
    Ckgen_ClkIdType Clk )
```

Get can clock division.

Note

Function ID: DES_CKGEN_API_221

Parameters

in	Clk	clock id,value can be one of the list value
		<ul style="list-style-type: none">• CKGEN_CAN0_CLK [40][42][43]• CKGEN_CAN1_CLK [40][42][43]• CKGEN_CAN2_CLK [40][42][43]• CKGEN_CAN3_CLK [40][42][43]• CKGEN_CAN4_CLK [42][43]• CKGEN_CAN5_CLK [42][43]

Returns

uint8: clock division

Definition at line 118 of file AC784xx_Ckgen_Reg.c.

4.2.2.2 Ckgen_Reg_GetCanClkMux()

```
Ckgen_ClkIdType Ckgen_Reg_GetCanClkMux (
    Ckgen_ClkIdType Clk )
```

Get can clock mux.

get can clock mux

Note

Function ID: DES_CKGEN_API_200

Parameters

<i>in</i>	<i>Clk</i>	clock id, value can be one of the list value
		<ul style="list-style-type: none"> • CKGEN_CAN0_CLK [40][42][43] • CKGEN_CAN1_CLK [40][42][43] • CKGEN_CAN2_CLK [40][42][43] • CKGEN_CAN3_CLK [40][42][43] • CKGEN_CAN4_CLK [42][43] • CKGEN_CAN5_CLK [42][43]

Returns

Ckgen_ClkIdType: mux clock id

- CKGEN_OFF_CLK [40][42][43]
- CKGEN_HSE_DIV2_CLK [40][42][43]
- CKGEN_SYS_CLK [40][42][43]
- CKGEN_VHSI_DIV2_CLK [40][42][43]
- CKGEN_SPLL_DIV2_CLK [40][42][43]

Definition at line 1149 of file AC784xx_Ckgen_Reg.c.

4.2.2.3 Ckgen_Reg_GetClkoutClkMux()

```
Ckgen_ClkIdType Ckgen_Reg_GetClkoutClkMux (
    void )
```

get clockout mux

Note

Function ID: DES_CKGEN_API_206

Returns

Ckgen_ClkIdType: mux clock id

- CKGEN_HSE_CLK [40][42][43]
- CKGEN_HSI_CLK [40][43]
- CKGEN_VHSI_CLK [40][42][43]
- CKGEN_SPLL_CLK [40][42][43]
- CKGEN_FLASH_CLK [40][42][43]
- CKGEN_RTC_CLK [40]
- CKGEN_LSI_CLK [40][42][43]
- CKGEN_LSI_128K_CLK [40][42][43]
- CKGEN_HSE_DIV2_CLK [40][42][43]
- CKGEN_VHSI_DIV2_CLK [40][42][43]

- CKGEN_HSI_DIV2_CLK [40][43]
- CKGEN_SPLL_DIV2_CLK [40][42][43]
- CKGEN_BUS_CLK [40][42][43]
- CKGEN_SYS_CLK [40][42][43]
- CKGEN_ADC_SPLLDIV_CLK [43]
- CKGEN_HSE_DIV1_CLK [42][43]
- CKGEN_VHSI_DIV1_CLK [42][43]
- CKGEN_HSI_DIV1_CLK [43]
- CKGEN_SPLL_DIV1_CLK [42][43]

Definition at line 758 of file AC784xx_Ckgen_Reg.c.

4.2.2.4 Ckgen_Reg_GetCommPeriphClkMux()

```
Ckgen_ClkIdType Ckgen_Reg_GetCommPeriphClkMux (
    Ckgen_ClkIdType Clk )
```

get common peripheral clock mux

Note

Function ID: DES_CKGEN_API_202

Parameters

<i>in</i>	<i>Clk</i>	clock id, value can be one of the list value <ul style="list-style-type: none"> • CKGEN_I2C0_CLK [40][42][43] • CKGEN_I2C1_CLK [42][43] • CKGEN_I2C2_CLK [43] • CKGEN_TIMER_CLK [40][42][43] • CKGEN_SPI0_CLK [40][42][43] • CKGEN_SPI1_CLK [40][42][43] • CKGEN_SPI2_CLK [40][42][43] • CKGEN_SPI3_CLK [42][43] • CKGEN_SPI4_CLK [43] • CKGEN_ADC0_CLK [40][42][43] • CKGEN_ADC1_CLK [40][42][43] • CKGEN_PCT_CLK [40][43] • CKGEN_EIO_CLK [40][42][43] • CKGEN_UART0_CLK [40][42][43] • CKGEN_UART1_CLK [40][42][43] • CKGEN_UART2_CLK [40][42][43] • CKGEN_UART3_CLK [40][42][43] • CKGEN_UART4_CLK [43] • CKGEN_UART5_CLK [43] • CKGEN_UART6_CLK [43] • CKGEN_UART7_CLK [43]
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Returns

Ckgen_ClkIdType: mux clock id

- CKGEN_OFF_CLK [40][42][43]
- CKGEN_HSE_DIV2_CLK [40][42][43]
- CKGEN_HSI_DIV2_CLK [40][42][43]
- CKGEN_VHSI_DIV2_CLK [40][42][43]
- CKGEN_SPLL_DIV2_CLK [40][42][43]
- CKGEN_ADC_SPLLDIV_CLK [43]

Definition at line 1004 of file AC784xx_Ckgen_Reg.c.

4.2.2.5 Ckgen_Reg_GetPwmClkMux()

```
Ckgen_ClkIdType Ckgen_Reg_GetPwmClkMux (  
    Ckgen_ClkIdType Clk )
```

Get pwm clock mux.

get pwm clock mux

Note

Function ID: DES_CKGEN_API_201

Parameters

in	Clk	clock id, value can be one of the list value
		<ul style="list-style-type: none">• CKGEN_PWM0_CLK [40][42][43]• CKGEN_PWM1_CLK [40][42][43]• CKGEN_PWM2_CLK [40][42][43]• CKGEN_PWM3_CLK [40][42][43]• CKGEN_PWM4_CLK [40][42][43]• CKGEN_PWM5_CLK [40][42][43]• CKGEN_PWM6_CLK [43]• CKGEN_PWM7_CLK [43]

Returns

- Ckgen_ClkIdType: mux clock id
- CKGEN_HSE_DIV1_CLK [40][42][43]
 - CKGEN_HSI_DIV1_CLK [40][42][43]
 - CKGEN_VHSI_DIV1_CLK [40][42][43]
 - CKGEN_SPLL_DIV1_CLK [40][42][43]
 - CKGEN_PWM_EXT_CLK0 [40][42][43]
 - CKGEN_PWM_EXT_CLK1 [40][42][43]
 - CKGEN_PWM_EXT_CLK2 [40][42][43]

Definition at line 1099 of file AC784xx_Ckgen_Reg.c.

4.2.2.6 Ckgen_Reg_GetSPLLClkMux()

```
Ckgen_ClkIdType Ckgen_Reg_GetSPLLClkMux (  
    void )
```

get spll mux

Note

Function ID: DES_CKGEN_API_208

Returns

- Ckgen_ClkIdType: mux clock id
- CKGEN_HSI_CLK [40][43]
 - CKGEN_VHSI_CLK [42]
 - CKGEN_HSE_CLK [40][42][43]

Definition at line 686 of file AC784xx_Ckgen_Reg.c.

4.2.2.7 Ckgen_Reg_SetCanClkDiv()

```
void Ckgen_Reg_SetCanClkDiv (
    Ckgen_ClkIdType Clk,
    uint8 Div )
```

Set can clock division.

Note

Function ID: DES_CKGEN_API_223

Parameters

in	Clk	clock id,value can be one of the list value <ul style="list-style-type: none">• CKGEN_CAN0_CLK [40][42][43]• CKGEN_CAN1_CLK [40][42][43]• CKGEN_CAN2_CLK [40][42][43]• CKGEN_CAN3_CLK [40][42][43]• CKGEN_CAN4_CLK [42][43]• CKGEN_CAN5_CLK [42][43]
in	Div	clock division

Returns

void

Definition at line 66 of file AC784xx_Ckgen_Reg.c.

4.2.2.8 Ckgen_Reg_SetCanClkMux()

```
void Ckgen_Reg_SetCanClkMux (
    Ckgen_ClkIdType Clk,
    Ckgen_ClkIdType ClkSrc )
```

Set can clock mux.

Note

Function ID: DES_CKGEN_API_203

Parameters

in	Clk	clock id, value can be one of the list value <ul style="list-style-type: none">• CKGEN_CAN0_CLK [40][42][43]• CKGEN_CAN1_CLK [40][42][43]• CKGEN_CAN2_CLK [40][42][43]• CKGEN_CAN3_CLK [40][42][43]• CKGEN_CAN4_CLK [42][43]• CKGEN_CAN5_CLK [42][43]
in	ClkSrc	clock id, value can be one of the list value <ul style="list-style-type: none">• CKGEN_OFF_CLK [40][42][43]• CKGEN_HSE_DIV2_CLK [40][42][43]• CKGEN_SYS_CLK [40][42][43]• CKGEN_VHSI_DIV2_CLK [40][42][43]• CKGEN_SPLL_DIV2_CLK [40][42][43]

Returns

void

Definition at line 952 of file AC784xx_Ckgen_Reg.c.

4.2.2.9 Ckgen_Reg_SetClkoutClkMux()

```
void Ckgen_Reg_SetClkoutClkMux (
    Ckgen_ClkIdType ClkSrc )
```

Set clkout clock mux.

Note

Function ID: DES_CKGEN_API_207

Parameters

in	<i>ClkSrc</i>	clock source id, value can be one of the list value <ul style="list-style-type: none"> • CKGEN_HSE_CLK [40][42][43] • CKGEN_HSI_CLK [40][43] • CKGEN_VHSI_CLK [40][42][43] • CKGEN_SPLL_CLK [40][42][43] • CKGEN_FLASH_CLK [40][42][43] • CKGEN_RTC_CLK [40] • CKGEN_LSI_CLK [40][42][43] • CKGEN_LSI_128K_CLK [40][42][43] • CKGEN_HSE_DIV2_CLK [40][42][43] • CKGEN_VHSI_DIV2_CLK [40][42][43] • CKGEN_HSI_DIV2_CLK [40][43] • CKGEN_SPLL_DIV2_CLK [40][42][43] • CKGEN_BUS_CLK [40][42][43] • CKGEN_SYS_CLK [40][42][43] • CKGEN_ADC_SPLLDIV_CLK [43] • CKGEN_HSE_DIV1_CLK [42][43] • CKGEN_VHSI_DIV1_CLK [42][43] • CKGEN_HSI_DIV1_CLK [43] • CKGEN_SPLL_DIV1_CLK [42][43]
----	---------------	---

Returns

void

Definition at line 722 of file AC784xx_Ckgen_Reg.c.

4.2.2.10 Ckgen_Reg_SetCommPeriphClkMux()

```
void Ckgen_Reg_SetCommPeriphClkMux (
    Ckgen_ClkIdType Clk,
    Ckgen_ClkIdType ClkSrc )
```

Set common peripheral clkout clock mux.

Set common peripheral clock mux.

Note

Function ID: DES_CKGEN_API_205

Parameters

in	Clk	<p>clock id, value can be one of the list value</p> <ul style="list-style-type: none"> • CKGEN_I2C0_CLK [40][42][43] • CKGEN_I2C1_CLK [42][43] • CKGEN_I2C2_CLK [43] • CKGEN_TIMER_CLK [40][42][43] • CKGEN_SPI0_CLK [40][42][43] • CKGEN_SPI1_CLK [40][42][43] • CKGEN_SPI2_CLK [40][42][43] • CKGEN_SPI3_CLK [42][43] • CKGEN_SPI4_CLK [43] • CKGEN_ADC0_CLK [40][42][43] • CKGEN_ADC1_CLK [40][42][43] • CKGEN_PCT_CLK [40][43] • CKGEN_EIO_CLK [40][42][43] • CKGEN_UART0_CLK [40][42][43] • CKGEN_UART1_CLK [40][42][43] • CKGEN_UART2_CLK [40][42][43] • CKGEN_UART3_CLK [40][42][43] • CKGEN_UART4_CLK [43] • CKGEN_UART5_CLK [43] • CKGEN_UART6_CLK [43] • CKGEN_UART7_CLK [43]
in	ClkSrc	<p>clock id, value can be one of the list value</p> <ul style="list-style-type: none"> • CKGEN_OFF_CLK [40][42][43] • CKGEN_HSE_DIV2_CLK [40][42][43] • CKGEN_HSI_DIV2_CLK [40][42][43] • CKGEN_VHSI_DIV2_CLK [40][42][43] • CKGEN_SPLL_DIV2_CLK [40][42][43] • CKGEN_ADC_SPLLDIV_CLK [43]

Returns

void

Definition at line 807 of file AC784xx_Ckgen_Reg.c.

4.2.2.11 Ckgen_Reg_SetPwmClkMux()

```
void Ckgen_Reg_SetPwmClkMux (
    Ckgen_ClkIdType Clk,
    Ckgen_ClkIdType ClkSrc )
```

Set pwm clock mux.

Note

Function ID: DES_CKGEN_API_204

Parameters

in	<i>Clk</i>	clock id, value can be one of the list value <ul style="list-style-type: none"> • CKGEN_PWM0_CLK [40][42][43] • CKGEN_PWM1_CLK [40][42][43] • CKGEN_PWM2_CLK [40][42][43] • CKGEN_PWM3_CLK [40][42][43] • CKGEN_PWM4_CLK [40][42][43] • CKGEN_PWM5_CLK [40][42][43] • CKGEN_PWM6_CLK [43] • CKGEN_PWM7_CLK [43]
in	<i>ClkSrc</i>	clock id, value can be one of the list value <ul style="list-style-type: none"> • CKGEN_HSE_DIV1_CLK [40][42][43] • CKGEN_HSI_DIV1_CLK [40][42][43] • CKGEN_VHSI_DIV1_CLK [40][42][43] • CKGEN_SPLL_DIV1_CLK [40][42][43] • CKGEN_PWM_EXT_CLK0 [40][42][43] • CKGEN_PWM_EXT_CLK1 [40][42][43] • CKGEN_PWM_EXT_CLK2 [40][42][43]

Returns

void

Definition at line 904 of file AC784xx_Ckgen_Reg.c.

4.2.2.12 Ckgen_Reg_SetSPLLClkMux()

```
void Ckgen_Reg_SetSPLLClkMux (
    Ckgen_ClkIdType ClkSrc )
```

Set spll clock mux.

Note

Function ID: DES_CKGEN_API_209

Parameters

in	ClkSrc	clock source id, value can be one of the list value <ul style="list-style-type: none"> • CKGEN_HSI_CLK [40][43] • CKGEN_VHSI_CLK [42] • CKGEN_HSE_CLK [40][42][43]
----	--------	---

Returns

void

Definition at line 668 of file AC784xx_Ckgen_Reg.c.

4.3 AC784xx_Ckgen_Reg.h File Reference

This file provides read/write CKGEN hardware registers.

```
#include "Device_Register.h"
```

Macros

- #define [CKGEN_REG_BASE](#) (CKGEN_BASE)

Functions

- LOCAL_INLINE void [Ckgen_Reg_SetRunModeBusClkDiv](#) (uint8 Div)
Set bus clock division in run mode.
- LOCAL_INLINE uint8 [Ckgen_Reg_GetRunModeBusClkDiv](#) (void)
Get bus clock division in run mode.
- LOCAL_INLINE void [Ckgen_Reg_SetRunModeSysClkDiv](#) (uint8 Div)
Set system clock division in run mode.
- LOCAL_INLINE uint8 [Ckgen_Reg_GetRunModeSysClkDiv](#) (void)
Get system clock division in run mode.
- LOCAL_INLINE void [Ckgen_Reg_SetRunModeSysClkSrc](#) (uint8 SysClkSrc)
Set system clock source in run mode.
- LOCAL_INLINE uint8 [Ckgen_Reg_GetRunModeSysClkSrc](#) (void)
Get system clock source in run mode.
- LOCAL_INLINE uint8 [Ckgen_Reg_GetPIIRefClk](#) (void)
Get pll reference clock.
- LOCAL_INLINE void [Ckgen_Reg_SetPIIRefClk](#) (uint32 PIIRefClk)
Set pll reference clock.
- LOCAL_INLINE void [Ckgen_Reg_EnableXOSCMonitor](#) (boolean IsEnable)
Enable XOSC monitor.

- LOCAL_INLINE void [Ckgen_Reg_EnableCTRLRegLock](#) (boolean IsEnable)
Enable CTRL reg lock.
- LOCAL_INLINE uint32 [Ana_Reg_GetPIIDivVal](#) (uint32 Mask, uint32 Pos)
Get pll clock division value.
- LOCAL_INLINE void [Ana_Reg_SetPIIDivVal](#) (uint32 Value, uint32 Mask, uint32 Pos)
Set pll clock division value.
- LOCAL_INLINE void [Ana_Reg_SetPIILockParam](#) (uint32 Value, uint32 Mask, uint32 Pos)
Set pll clock lock parameter.
- LOCAL_INLINE void [Ckgen_Reg_SetClkSrcDiv1](#) (uint32 Value, uint32 Mask, uint32 Pos)
Set clock source div1 division.
- LOCAL_INLINE void [Ckgen_Reg_SetClkSrcDiv2](#) (uint32 Value, uint32 Mask, uint32 Pos)
Set clock source div2 division.
- LOCAL_INLINE uint8 [Ckgen_Reg_GetClkSrcDiv1](#) (uint32 Mask, uint32 Pos)
Get clock source div1 division.
- LOCAL_INLINE uint8 [Ckgen_Reg_GetClkSrcDiv2](#) (uint32 Mask, uint32 Pos)
Get clock source div2 division.
- LOCAL_INLINE void [Ckgen_Reg_SetClkMux](#) (uint32 Offset, uint32 Value, uint32 Mask, uint32 Pos)
Set clock mux.
- LOCAL_INLINE uint8 [Ckgen_Reg_GetClkMux](#) (uint32 Offset, uint32 Mask, uint32 Pos)
Get clock mux.
- LOCAL_INLINE void [Ckgen_Reg_SetClkDiv](#) (uint32 Offset, uint32 Value, uint32 Mask, uint32 Pos)
Set clock division.
- LOCAL_INLINE uint8 [Ckgen_Reg_GetClkDiv](#) (uint32 Offset, uint32 Mask, uint32 Pos)
Get clock division.
- LOCAL_INLINE void [Ckgen_Reg_SetPeriphEnable](#) (uint32 Periph, boolean Enable)
Enable/Disbale Periph clock.
- LOCAL_INLINE boolean [Ckgen_Reg_GetPeriphEnable](#) (uint32 Periph)
Get Periph clock enable status.
- LOCAL_INLINE void [Ckgen_Reg_EnableClkout](#) (uint8 Enable)
Enable/Disbale clkout output.
- LOCAL_INLINE void [Ckgen_Reg_SetLPMux](#) (uint32 Val)
Set low power clock mux.
- LOCAL_INLINE uint32 [Ckgen_Reg_GetLSIMux](#) (void)
Get Isi clock mux.
- LOCAL_INLINE uint32 [Ckgen_Reg_GetPCTClkDiv](#) (void)
Get PCT clock divider.
- LOCAL_INLINE void [Ckgen_Reg_SetPCTClkDiv](#) (uint32 Div)
Set PCT clock divider.
- LOCAL_INLINE uint32 [Ckgen_Reg_GetTPIUClkDiv](#) (void)
Get TPIU clock divider.
- LOCAL_INLINE void [Ckgen_Reg_SetTPIUClkDiv](#) (uint32 Div)
Set TPIU clock divider.
- LOCAL_INLINE uint32 [Ckgen_Reg_GetClkoutClkDiv](#) (void)
Get clockout clock divider.
- LOCAL_INLINE void [Ckgen_Reg_SetClkoutClkDiv](#) (uint32 Div)
Set clockout clock divider.
- LOCAL_INLINE uint32 [Ckgen_Reg_GetSPLLDIV1ClkDiv](#) (void)
Get SPLLD div1 clock divider.
- LOCAL_INLINE void [Ckgen_Reg_SetSPLLDIV1ClkDiv](#) (uint32 Div)
Set SPLLD div1 clock divider.
- LOCAL_INLINE uint32 [Ckgen_Reg_GetSPLLDIV2ClkDiv](#) (void)
Get SPLLD div2 clock divider.
- LOCAL_INLINE void [Ckgen_Reg_SetSPLLDIV2ClkDiv](#) (uint32 Div)

- Set SPLL div2 clock divider.*
- LOCAL_INLINE uint32 [Ckgen_Reg_GetHSEDIV1ClkDiv](#) (void)
- Get HSE div1 clock divider.*
- LOCAL_INLINE void [Ckgen_Reg_SetHSEDIV1ClkDiv](#) (uint32 Div)
- Set HSE div1 clock divider.*
- LOCAL_INLINE uint32 [Ckgen_Reg_GetHSEDIV2ClkDiv](#) (void)
- Get HSE div2 clock divider.*
- LOCAL_INLINE void [Ckgen_Reg_SetHSEDIV2ClkDiv](#) (uint32 Div)
- Set HSE div2 clock divider.*
- LOCAL_INLINE uint32 [Ckgen_Reg_GetVHSIDIV1ClkDiv](#) (void)
- Get VHSI div1 clock divider.*
- LOCAL_INLINE void [Ckgen_Reg_SetVHSIDIV1ClkDiv](#) (uint32 Div)
- Set VHSI div1 clock divider.*
- LOCAL_INLINE uint32 [Ckgen_Reg_GetVHSIDIV2ClkDiv](#) (void)
- Get VHSI div2 clock divider.*
- LOCAL_INLINE void [Ckgen_Reg_SetVHSIDIV2ClkDiv](#) (uint32 Div)
- Set VHSI div2 clock divider.*
- LOCAL_INLINE uint32 [Ckgen_Reg_GetHSIDIV1ClkDiv](#) (void)
- Get HSI div1 clock divider.*
- LOCAL_INLINE void [Ckgen_Reg_SetHSIDIV1ClkDiv](#) (uint32 Div)
- Set HSI div1 clock divider.*
- LOCAL_INLINE uint32 [Ckgen_Reg_GetHSIDIV2ClkDiv](#) (void)
- Get HSI div2 clock divider.*
- LOCAL_INLINE void [Ckgen_Reg_SetHSIDIV2ClkDiv](#) (uint32 Div)
- Set HSI div2 clock divider.*
- Ckgen_ClkIdType [Ckgen_Reg_GetCanClkMux](#) (Ckgen_ClkIdType Clk)
- get can clock mux*
- Ckgen_ClkIdType [Ckgen_Reg_GetPwmClkMux](#) (Ckgen_ClkIdType Clk)
- get pwm clock mux*
- Ckgen_ClkIdType [Ckgen_Reg_GetCommPeriphClkMux](#) (Ckgen_ClkIdType Clk)
- get common peripheral clock mux*
- void [Ckgen_Reg_SetCanClkMux](#) (Ckgen_ClkIdType Clk, Ckgen_ClkIdType ClkSrc)
- Set can clock mux.*
- void [Ckgen_Reg_SetPwmClkMux](#) (Ckgen_ClkIdType Clk, Ckgen_ClkIdType ClkSrc)
- Set pwm clock mux.*
- void [Ckgen_Reg_SetCommPeriphClkMux](#) (Ckgen_ClkIdType Clk, Ckgen_ClkIdType ClkSrc)
- Set common peripheral clock mux.*
- Ckgen_ClkIdType [Ckgen_Reg_GetClkoutClkMux](#) (void)
- get clockout mux*
- void [Ckgen_Reg_SetClkoutClkMux](#) (Ckgen_ClkIdType ClkSrc)
- Set clkout clock mux.*
- Ckgen_ClkIdType [Ckgen_Reg_GetSPLLClkMux](#) (void)
- get spll mux*
- void [Ckgen_Reg_SetSPLLClkMux](#) (Ckgen_ClkIdType ClkSrc)
- Set spll clock mux.*
- uint8 [Ckgen_Reg_GetCanClkDiv](#) (Ckgen_ClkIdType Clk)
- Get can clock division.*
- void [Ckgen_Reg_SetCanClkDiv](#) (Ckgen_ClkIdType Clk, uint8 Div)
- Set can clock division.*
- LOCAL_INLINE uint32 [Ana_Reg_GetPllPosDivVal](#) (void)
- Get posdivider value.*
- LOCAL_INLINE void [Ana_Reg_SetPllPosDivVal](#) (uint32 Div)
- Set pll posdivider value.*

- LOCAL_INLINE uint32 [Ana_Reg_GetPllPreDivVal](#) (void)
Get predivider value.
- LOCAL_INLINE void [Ana_Reg_SetPllPreDivVal](#) (uint32 Div)
Set pll predivider value.
- LOCAL_INLINE uint32 [Ana_Reg_GetPllFbkDivVal](#) (void)
Get fbkdivider value.
- LOCAL_INLINE void [Ana_Reg_SetPllFbkDivVal](#) (uint32 Div)
Set pll fbkdivider value.

4.3.1 Detailed Description

This file provides read/write CKGEN hardware registers.

4.3.2 Macro Definition Documentation

4.3.2.1 CKGEN_REG_BASE

```
#define CKGEN_REG_BASE (CKGEN_BASE)
```

Definition at line 56 of file AC784xx_Ckgen_Reg.h.

4.3.3 Function Documentation

4.3.3.1 Ana_Reg_GetPllDivVal()

```
LOCAL_INLINE uint32 Ana_Reg_GetPllDivVal (  
    uint32 Mask,  
    uint32 Pos )
```

Get pll clock division value.

Note

Function ID: DES_CKGEN_API_315

Parameters

in	<i>Mask</i>	register value mask
in	<i>Pos</i>	register position

Returns

uint32: pll clock division value

Definition at line 242 of file AC784xx_Ckgen_Reg.h.

4.3.3.2 Ana_Reg_GetPIIFbkDivVal()

```
LOCAL_INLINE uint32 Ana_Reg_GetPllFbkDivVal (  
    void )
```

Get fbkdivider value.

Note

Function ID: DES_CKGEN_API_360

Returns

uint32: fbkdivider

Definition at line 1084 of file AC784xx_Ckgen_Reg.h.

4.3.3.3 Ana_Reg_GetPIIPosDivVal()

```
LOCAL_INLINE uint32 Ana_Reg_GetPllPosDivVal (  
    void )
```

Get posdivider value.

Note

Function ID: DES_CKGEN_API_356

Returns

uint32: posdivider

Definition at line 1042 of file AC784xx_Ckgen_Reg.h.

4.3.3.4 Ana_Reg_GetPlIPreDivVal()

```
LOCAL_INLINE uint32 Ana_Reg_GetPlIPreDivVal (
    void )
```

Get predivider value.

Note

Function ID: DES_CKGEN_API_358

Returns

uint32: predivider

Definition at line 1063 of file AC784xx_Ckgen_Reg.h.

4.3.3.5 Ana_Reg_SetPlIDivVal()

```
LOCAL_INLINE void Ana_Reg_SetPlIDivVal (
    uint32 Value,
    uint32 Mask,
    uint32 Pos )
```

Set pll clock division value.

Note

Function ID: DES_CKGEN_API_316

Parameters

in	<i>Value</i>	division value to set
in	<i>Mask</i>	register value mask
in	<i>Pos</i>	register position

Returns

void

Definition at line 255 of file AC784xx_Ckgen_Reg.h.

4.3.3.6 Ana_Reg_SetPlIFbkDivVal()

```
LOCAL_INLINE void Ana_Reg_SetPlIFbkDivVal (
    uint32 Div )
```

Set pll fbkdivider value.

Note

Function ID: DES_CKGEN_API_361

Parameters

in	<i>Div</i>	division value to set
----	------------	-----------------------

Returns

void

Definition at line 1095 of file AC784xx_Ckgen_Reg.h.

4.3.3.7 Ana_Reg_SetPllLockParam()

```
LOCAL_INLINE void Ana_Reg_SetPllLockParam (
    uint32 Value,
    uint32 Mask,
    uint32 Pos )
```

Set pll clock lock parameter.

Note

Function ID: DES_CKGEN_API_317

Parameters

in	<i>Value</i>	value to set
in	<i>Mask</i>	register value mask
in	<i>Pos</i>	register position

Returns

void

Definition at line 268 of file AC784xx_Ckgen_Reg.h.

4.3.3.8 Ana_Reg_SetPllPosDivVal()

```
LOCAL_INLINE void Ana_Reg_SetPllPosDivVal (
    uint32 Div )
```

Set pll posdivider value.

Note

Function ID: DES_CKGEN_API_357

Parameters

<i>in</i>	<i>Div</i>	division value to set
-----------	------------	-----------------------

Returns

void

Definition at line 1053 of file AC784xx_Ckgen_Reg.h.

4.3.3.9 Ana_Reg_SetPlIPreDivVal()

```
LOCAL_INLINE void Ana_Reg_SetPlIPreDivVal (
    uint32 Div )
```

Set pll predivider value.

Note

Function ID: DES_CKGEN_API_359

Parameters

<i>in</i>	<i>Div</i>	division value to set
-----------	------------	-----------------------

Returns

void

Definition at line 1074 of file AC784xx_Ckgen_Reg.h.

4.3.3.10 Ckgen_Reg_EnableClkout()

```
LOCAL_INLINE void Ckgen_Reg_EnableClkout (
    uint8 Enable )
```

Enable/Disable clkout output.

Note

Function ID: DES_CKGEN_API_328

Parameters

<i>in</i>	<i>Enable</i>	enable or disable
-----------	---------------	-------------------

Returns

void

Definition at line 431 of file AC784xx_Ckgen_Reg.h.

4.3.3.11 Ckgen_Reg_EnableCTRLRegLock()

```
LOCAL_INLINE void Ckgen_Reg_EnableCTRLRegLock (
    boolean IsEnable )
```

Enable CTRL reg lock.

Note

Function ID: DES_CKGEN_API_314

Parameters

<i>in</i>	<i>IsEnable</i>	TRUE is enable, FALSE is disable
-----------	-----------------	----------------------------------

Returns

void

Definition at line 229 of file AC784xx_Ckgen_Reg.h.

4.3.3.12 Ckgen_Reg_EnableXOSCMonitor()

```
LOCAL_INLINE void Ckgen_Reg_EnableXOSCMonitor (
    boolean IsEnable )
```

Enable XOSC monitor.

Note

Function ID: DES_CKGEN_API_313

Parameters

<i>in</i>	<i>IsEnable</i>	TRUE is enable, FALSE is disable
-----------	-----------------	----------------------------------

Returns

void

Definition at line 217 of file AC784xx_Ckgen_Reg.h.

4.3.3.13 Ckgen_Reg_GetCanClkDiv()

```
uint8 Ckgen_Reg_GetCanClkDiv (
    Ckgen_ClkIdType Clk )
```

Get can clock division.

Note

Function ID: DES_CKGEN_API_221

Parameters

in	Clk	clock id,value can be one of the list value
		<ul style="list-style-type: none">• CKGEN_CAN0_CLK [40][42][43]• CKGEN_CAN1_CLK [40][42][43]• CKGEN_CAN2_CLK [40][42][43]• CKGEN_CAN3_CLK [40][42][43]• CKGEN_CAN4_CLK [42][43]• CKGEN_CAN5_CLK [42][43]

Returns

uint8: clock division

Definition at line 118 of file AC784xx_Ckgen_Reg.c.

4.3.3.14 Ckgen_Reg_GetCanClkMux()

```
Ckgen_ClkIdType Ckgen_Reg_GetCanClkMux (
    Ckgen_ClkIdType Clk )
```

get can clock mux

Note

Function ID: DES_CKGEN_API_200

Parameters

<i>in</i>	<i>Clk</i>	clock id, value can be one of the list value <ul style="list-style-type: none"> • CKGEN_CAN0_CLK [40][42][43] • CKGEN_CAN1_CLK [40][42][43] • CKGEN_CAN2_CLK [40][42][43] • CKGEN_CAN3_CLK [40][42][43] • CKGEN_CAN4_CLK [42][43] • CKGEN_CAN5_CLK [42][43]
-----------	------------	---

Returns

Ckgen_ClkIdType: mux clock id

- CKGEN_OFF_CLK [40][42][43]
- CKGEN_HSE_DIV2_CLK [40][42][43]
- CKGEN_SYS_CLK [40][42][43]
- CKGEN_VHSI_DIV2_CLK [40][42][43]
- CKGEN_SPLL_DIV2_CLK [40][42][43]

get can clock mux

Note

Function ID: DES_CKGEN_API_200

Parameters

<i>in</i>	<i>Clk</i>	clock id, value can be one of the list value <ul style="list-style-type: none"> • CKGEN_CAN0_CLK [40][42][43] • CKGEN_CAN1_CLK [40][42][43] • CKGEN_CAN2_CLK [40][42][43] • CKGEN_CAN3_CLK [40][42][43] • CKGEN_CAN4_CLK [42][43] • CKGEN_CAN5_CLK [42][43]
-----------	------------	---

Returns

Ckgen_ClkIdType: mux clock id

- CKGEN_OFF_CLK [40][42][43]
- CKGEN_HSE_DIV2_CLK [40][42][43]
- CKGEN_SYS_CLK [40][42][43]
- CKGEN_VHSI_DIV2_CLK [40][42][43]
- CKGEN_SPLL_DIV2_CLK [40][42][43]

Definition at line 1149 of file AC784xx_Ckgen_Reg.c.

4.3.3.15 Ckgen_Reg_GetClkDiv()

```
LOCAL_INLINE uint8 Ckgen_Reg_GetClkDiv (
    uint32 Offset,
    uint32 Mask,
    uint32 Pos )
```

Get clock division.

Note

Function ID: DES_CKGEN_API_325

Parameters

in	<i>Offset</i>	clock idx offset
in	<i>Mask</i>	register value mask
in	<i>Pos</i>	register position

Returns

uint8: clock division

Definition at line 386 of file AC784xx_Ckgen_Reg.h.

4.3.3.16 Ckgen_Reg_GetClkMux()

```
LOCAL_INLINE uint8 Ckgen_Reg_GetClkMux (
    uint32 Offset,
    uint32 Mask,
    uint32 Pos )
```

Get clock mux.

Note

Function ID: DES_CKGEN_API_323

Parameters

in	<i>Offset</i>	clock idx offset
in	<i>Mask</i>	register value mask
in	<i>Pos</i>	register position

Returns

uint8: clock mux

Definition at line 355 of file AC784xx_Ckgen_Reg.h.

4.3.3.17 Ckgen_Reg_GetClkoutClkDiv()

```
LOCAL_INLINE uint32 Ckgen_Reg_GetClkoutClkDiv (
    void )
```

Get clockout clock divider.

Note

Function ID: DES_CKGEN_API_338

Returns

uint32: clockout clock divider

Definition at line 544 of file AC784xx_Ckgen_Reg.h.

4.3.3.18 Ckgen_Reg_GetClkoutClkMux()

```
Ckgen_ClkIdType Ckgen_Reg_GetClkoutClkMux (
    void )
```

get clockout mux

Note

Function ID: DES_CKGEN_API_206

Returns

Ckgen_ClkIdType: mux clock id

- CKGEN_HSE_CLK [40][42][43]
- CKGEN_HSI_CLK [40][43]
- CKGEN_VHSI_CLK [40][42][43]
- CKGEN_SPLL_CLK [40][42][43]
- CKGEN_FLASH_CLK [40][42][43]
- CKGEN_RTC_CLK [40]
- CKGEN_LSI_CLK [40][42][43]
- CKGEN_LSI_128K_CLK [40][42][43]
- CKGEN_HSE_DIV2_CLK [40][42][43]
- CKGEN_VHSI_DIV2_CLK [40][42][43]
- CKGEN_HSI_DIV2_CLK [40][43]
- CKGEN_SPLL_DIV2_CLK [40][42][43]
- CKGEN_BUS_CLK [40][42][43]
- CKGEN_SYS_CLK [40][42][43]
- CKGEN_ADC_SPLLDIV_CLK [43]
- CKGEN_HSE_DIV1_CLK [42][43]
- CKGEN_VHSI_DIV1_CLK [42][43]
- CKGEN_HSI_DIV1_CLK [43]
- CKGEN_SPLL_DIV1_CLK [42][43]

Definition at line 758 of file AC784xx_Ckgen_Reg.c.

4.3.3.19 Ckgen_Reg_GetClkSrcDiv1()

```
LOCAL_INLINE uint8 Ckgen_Reg_GetClkSrcDiv1 (
    uint32 Mask,
    uint32 Pos )
```

Get clock source div1 division.

Note

Function ID: DES_CKGEN_API_320

Parameters

in	<i>Mask</i>	register value mask
in	<i>Pos</i>	register position

Returns

uint8: clock source div1 division

Definition at line 310 of file AC784xx_Ckgen_Reg.h.

4.3.3.20 Ckgen_Reg_GetClkSrcDiv2()

```
LOCAL_INLINE uint8 Ckgen_Reg_GetClkSrcDiv2 (
    uint32 Mask,
    uint32 Pos )
```

Get clock source div2 division.

Note

Function ID: DES_CKGEN_API_321

Parameters

in	<i>Mask</i>	register value mask
in	<i>Pos</i>	register position

Returns

uint8: clock source div2 division

Definition at line 324 of file AC784xx_Ckgen_Reg.h.

4.3.3.21 Ckgen_Reg_GetCommPeriphClkMux()

```
Ckgen_ClkIdType Ckgen_Reg_GetCommPeriphClkMux (
    Ckgen_ClkIdType Clk )
```

get common peripheral clock mux

Note

Function ID: DES_CKGEN_API_202

Parameters

in	Clk	clock id, value can be one of the list value
		<ul style="list-style-type: none">• CKGEN_I2C0_CLK [40][42][43]• CKGEN_I2C1_CLK [42][43]• CKGEN_I2C2_CLK [43]• CKGEN_TIMER_CLK [40][42][43]• CKGEN_SPI0_CLK [40][42][43]• CKGEN_SPI1_CLK [40][42][43]• CKGEN_SPI2_CLK [40][42][43]• CKGEN_SPI3_CLK [42][43]• CKGEN_SPI4_CLK [43]• CKGEN_ADC0_CLK [40][42][43]• CKGEN_ADC1_CLK [40][42][43]• CKGEN_PCT_CLK [40][43]• CKGEN_EIO_CLK [40][42][43]• CKGEN_UART0_CLK [40][42][43]• CKGEN_UART1_CLK [40][42][43]• CKGEN_UART2_CLK [40][42][43]• CKGEN_UART3_CLK [40][42][43]• CKGEN_UART4_CLK [43]• CKGEN_UART5_CLK [43]• CKGEN_UART6_CLK [43]• CKGEN_UART7_CLK [43]

Returns

- Ckgen_ClkIdType: mux clock id
- CKGEN_OFF_CLK [40][42][43]
 - CKGEN_HSE_DIV2_CLK [40][42][43]
 - CKGEN_HSI_DIV2_CLK [40][42][43]

- CKGEN_VHSI_DIV2_CLK [40][42][43]
- CKGEN_SPLL_DIV2_CLK [40][42][43]
- CKGEN_ADC_SPLLDIV_CLK [43]

Definition at line 1004 of file AC784xx_Ckgen_Reg.c.

4.3.3.22 Ckgen_Reg_GetHSEDIV1ClkDiv()

```
LOCAL_INLINE uint32 Ckgen_Reg_GetHSEDIV1ClkDiv (  
    void )
```

Get HSE div1 clock divider.

Note

Function ID: DES_CKGEN_API_344

Returns

uint32: HSE div1 clock divider

Definition at line 607 of file AC784xx_Ckgen_Reg.h.

4.3.3.23 Ckgen_Reg_GetHSEDIV2ClkDiv()

```
LOCAL_INLINE uint32 Ckgen_Reg_GetHSEDIV2ClkDiv (  
    void )
```

Get HSE div2 clock divider.

Note

Function ID: DES_CKGEN_API_346

Returns

uint32: HSE div2 clock divider

Definition at line 628 of file AC784xx_Ckgen_Reg.h.

4.3.3.24 Ckgen_Reg_GetHSIDIV1ClkDiv()

```
LOCAL_INLINE uint32 Ckgen_Reg_GetHSIDIV1ClkDiv (  
    void )
```

Get HSI div1 clock divider.

Note

Function ID: DES_CKGEN_API_352

Returns

uint32: HSI div1 clock divider

Definition at line 691 of file AC784xx_Ckgen_Reg.h.

4.3.3.25 Ckgen_Reg_GetHSIDIV2ClkDiv()

```
LOCAL_INLINE uint32 Ckgen_Reg_GetHSIDIV2ClkDiv (  
    void )
```

Get HSI div2 clock divider.

Note

Function ID: DES_CKGEN_API_354

Returns

uint32: HSI div2 clock divider

Definition at line 720 of file AC784xx_Ckgen_Reg.h.

4.3.3.26 Ckgen_Reg_GetLSIMux()

```
LOCAL_INLINE uint32 Ckgen_Reg_GetLSIMux (  
    void )
```

Get lsi clock mux.

Note

Function ID: DES_CKGEN_API_332

Returns

uint32: lsi clock mux

Definition at line 480 of file AC784xx_Ckgen_Reg.h.

4.3.3.27 Ckgen_Reg_GetPCTClkDiv()

```
LOCAL_INLINE uint32 Ckgen_Reg_GetPCTClkDiv (  
    void )
```

Get PCT clock divider.

Note

Function ID: DES_CKGEN_API_334

Returns

uint32: PCT clock divider

Definition at line 502 of file AC784xx_Ckgen_Reg.h.

4.3.3.28 Ckgen_Reg_GetPeriphEnable()

```
LOCAL_INLINE boolean Ckgen_Reg_GetPeriphEnable (  
    uint32 Periph )
```

Get Periph clock enable status.

Note

Function ID: DES_CKGEN_API_327

Parameters

in	<i>Periph</i>	peripheral id
----	---------------	---------------

Returns

uint8: clock enable status

Definition at line 416 of file AC784xx_Ckgen_Reg.h.

4.3.3.29 Ckgen_Reg_GetPllRefClk()

```
LOCAL_INLINE uint8 Ckgen_Reg_GetPllRefClk (  
    void )
```

Get pll reference clock.

Note

Function ID: DES_CKGEN_API_311

Returns

uint8: pll reference clock register value

Definition at line 195 of file AC784xx_Ckgen_Reg.h.

4.3.3.30 Ckgen_Reg_GetPwmClkMux()

```
Ckgen_ClkIdType Ckgen_Reg_GetPwmClkMux (
    Ckgen_ClkIdType Clk )
```

get pwm clock mux

Note

Function ID: DES_CKGEN_API_201

Parameters

in	Clk	clock id, value can be one of the list value
		<ul style="list-style-type: none">• CKGEN_PWM0_CLK [40][42][43]• CKGEN_PWM1_CLK [40][42][43]• CKGEN_PWM2_CLK [40][42][43]• CKGEN_PWM3_CLK [40][42][43]• CKGEN_PWM4_CLK [40][42][43]• CKGEN_PWM5_CLK [40][42][43]• CKGEN_PWM6_CLK [43]• CKGEN_PWM7_CLK [43]

Returns

Ckgen_ClkIdType: mux clock id

- CKGEN_HSE_DIV1_CLK [40][42][43]
- CKGEN_HSI_DIV1_CLK [40][42][43]
- CKGEN_VHSI_DIV1_CLK [40][42][43]
- CKGEN_SPLL_DIV1_CLK [40][42][43]
- CKGEN_PWM_EXT_CLK0 [40][42][43]
- CKGEN_PWM_EXT_CLK1 [40][42][43]
- CKGEN_PWM_EXT_CLK2 [40][42][43]

get pwm clock mux

Note

Function ID: DES_CKGEN_API_201

Parameters

in	Clk	clock id, value can be one of the list value
		<ul style="list-style-type: none">• CKGEN_PWM0_CLK [40][42][43]• CKGEN_PWM1_CLK [40][42][43]• CKGEN_PWM2_CLK [40][42][43]• CKGEN_PWM3_CLK [40][42][43]• CKGEN_PWM4_CLK [40][42][43]• CKGEN_PWM5_CLK [40][42][43]• CKGEN_PWM6_CLK [43]• CKGEN_PWM7_CLK [43]

Returns

Ckgen_ClkIdType: mux clock id

- CKGEN_HSE_DIV1_CLK [40][42][43]
- CKGEN_HSI_DIV1_CLK [40][42][43]
- CKGEN_VHSI_DIV1_CLK [40][42][43]
- CKGEN_SPLL_DIV1_CLK [40][42][43]
- CKGEN_PWM_EXT_CLK0 [40][42][43]
- CKGEN_PWM_EXT_CLK1 [40][42][43]
- CKGEN_PWM_EXT_CLK2 [40][42][43]

Definition at line 1099 of file AC784xx_Ckgen_Reg.c.

4.3.3.31 Ckgen_Reg_GetRunModeBusClkDiv()

```
LOCAL_INLINE uint8 Ckgen_Reg_GetRunModeBusClkDiv (
    void )
```

Get bus clock division in run mode.

Note

Function ID: DES_CKGEN_API_303

Returns

uint8: clock division value

Definition at line 107 of file AC784xx_Ckgen_Reg.h.

4.3.3.32 Ckgen_Reg_GetRunModeSysClkDiv()

```
LOCAL_INLINE uint8 Ckgen_Reg_GetRunModeSysClkDiv (  
    void )
```

Get system clock division in run mode.

Note

Function ID: DES_CKGEN_API_307

Returns

uint8: clock division value

Definition at line 150 of file AC784xx_Ckgen_Reg.h.

4.3.3.33 Ckgen_Reg_GetRunModeSysClkSrc()

```
LOCAL_INLINE uint8 Ckgen_Reg_GetRunModeSysClkSrc (  
    void )
```

Get system clock source in run mode.

Note

Function ID: DES_CKGEN_API_309

Returns

uint8: system clock source value

Definition at line 171 of file AC784xx_Ckgen_Reg.h.

4.3.3.34 Ckgen_Reg_GetSPLLClkMux()

```
Ckgen_ClkIdType Ckgen_Reg_GetSPLLClkMux (  
    void )
```

get spll mux

Note

Function ID: DES_CKGEN_API_208

Returns

Ckgen_ClkIdType: mux clock id

- CKGEN_HSI_CLK [40][43]
- CKGEN_VHSI_CLK [42]
- CKGEN_HSE_CLK [40][42][43]

Definition at line 686 of file AC784xx_Ckgen_Reg.c.

4.3.3.35 Ckgen_Reg_GetSPLLDIV1ClkDiv()

```
LOCAL_INLINE uint32 Ckgen_Reg_GetSPLLDIV1ClkDiv (  
    void )
```

Get SPLL div1 clock divider.

Note

Function ID: DES_CKGEN_API_340

Returns

uint32: SPLL div1 clock divider

Definition at line 565 of file AC784xx_Ckgen_Reg.h.

4.3.3.36 Ckgen_Reg_GetSPLLDIV2ClkDiv()

```
LOCAL_INLINE uint32 Ckgen_Reg_GetSPLLDIV2ClkDiv (  
    void )
```

Get SPLL div2 clock divider.

Note

Function ID: DES_CKGEN_API_342

Returns

uint32: SPLL div2 clock divider

Definition at line 586 of file AC784xx_Ckgen_Reg.h.

4.3.3.37 Ckgen_Reg_GetTPIUClkDiv()

```
LOCAL_INLINE uint32 Ckgen_Reg_GetTPIUClkDiv (  
    void )
```

Get TPIU clock divider.

Note

Function ID: DES_CKGEN_API_336

Returns

uint32: TPIU clock divider

Definition at line 523 of file AC784xx_Ckgen_Reg.h.

4.3.3.38 Ckgen_Reg_GetVHSIDIV1ClkDiv()

```
LOCAL_INLINE uint32 Ckgen_Reg_GetVHSIDIV1ClkDiv (  
    void )
```

Get VHSI div1 clock divider.

Note

Function ID: DES_CKGEN_API_348

Returns

uint32: VHSI div1 clock divider

Definition at line 649 of file AC784xx_Ckgen_Reg.h.

4.3.3.39 Ckgen_Reg_GetVHSIDIV2ClkDiv()

```
LOCAL_INLINE uint32 Ckgen_Reg_GetVHSIDIV2ClkDiv (  
    void )
```

Get VHSI div2 clock divider.

Note

Function ID: DES_CKGEN_API_350

Returns

uint32: VHSI div2 clock divider

Definition at line 670 of file AC784xx_Ckgen_Reg.h.

4.3.3.40 Ckgen_Reg_SetCanClkDiv()

```
void Ckgen_Reg_SetCanClkDiv (  
    Ckgen_ClkIdType Clk,  
    uint8 Div )
```

Set can clock division.

Note

Function ID: DES_CKGEN_API_223

Parameters

in	Clk	clock id,value can be one of the list value <ul style="list-style-type: none">• CKGEN_CAN0_CLK [40][42][43]• CKGEN_CAN1_CLK [40][42][43]• CKGEN_CAN2_CLK [40][42][43]• CKGEN_CAN3_CLK [40][42][43]• CKGEN_CAN4_CLK [42][43]• CKGEN_CAN5_CLK [42][43]
in	Div	clock division

Returns

void

Definition at line 66 of file AC784xx_Ckgen_Reg.c.

4.3.3.41 Ckgen_Reg_SetCanClkMux()

```
void Ckgen_Reg_SetCanClkMux (
    Ckgen_ClkIdType Clk,
    Ckgen_ClkIdType ClkSrc )
```

Set can clock mux.

Note

Function ID: DES_CKGEN_API_203

Parameters

in	Clk	clock id, value can be one of the list value <ul style="list-style-type: none">• CKGEN_CAN0_CLK [40][42][43]• CKGEN_CAN1_CLK [40][42][43]• CKGEN_CAN2_CLK [40][42][43]• CKGEN_CAN3_CLK [40][42][43]• CKGEN_CAN4_CLK [42][43]• CKGEN_CAN5_CLK [42][43]
in	ClkSrc	clock id, value can be one of the list value <ul style="list-style-type: none">• CKGEN_OFF_CLK [40][42][43]• CKGEN_HSE_DIV2_CLK [40][42][43]• CKGEN_SYS_CLK [40][42][43]• CKGEN_VHSI_DIV2_CLK [40][42][43]
Generated by Doxygen		<ul style="list-style-type: none">• CKGEN_SPLL_DIV2_CLK [40][42][43]

Returns

void

Definition at line 952 of file AC784xx_Ckgen_Reg.c.

4.3.3.42 Ckgen_Reg_SetClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetClkDiv (
    uint32 Offset,
    uint32 Value,
    uint32 Mask,
    uint32 Pos )
```

Set clock division.

Note

Function ID: DES_CKGEN_API_324

Parameters

in	<i>Offset</i>	clock idx offset
in	<i>Value</i>	value to set
in	<i>Mask</i>	register value mask
in	<i>Pos</i>	register position

Returns

void

Definition at line 371 of file AC784xx_Ckgen_Reg.h.

4.3.3.43 Ckgen_Reg_SetClkMux()

```
LOCAL_INLINE void Ckgen_Reg_SetClkMux (
    uint32 Offset,
    uint32 Value,
    uint32 Mask,
    uint32 Pos )
```

Set clock mux.

Note

Function ID: DES_CKGEN_API_322

Parameters

in	<i>Offset</i>	clock idx offset
in	<i>Value</i>	value to set
in	<i>Mask</i>	register value mask
in	<i>Pos</i>	register position

Returns

void

Definition at line 340 of file AC784xx_Ckgen_Reg.h.

4.3.3.44 Ckgen_Reg_SetClkoutClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetClkoutClkDiv (  
    uint32 Div )
```

Set clockout clock divider.

Note

Function ID: DES_CKGEN_API_339

Parameters

in	<i>Div</i>	division value to set
----	------------	-----------------------

Returns

void

Definition at line 555 of file AC784xx_Ckgen_Reg.h.

4.3.3.45 Ckgen_Reg_SetClkoutClkMux()

```
void Ckgen_Reg_SetClkoutClkMux (  
    Ckgen_ClkIdType ClkSrc )
```

Set clkout clock mux.

Note

Function ID: DES_CKGEN_API_207

Parameters

<i>in</i>	<i>ClkSrc</i>	clock source id, value can be one of the list value <ul style="list-style-type: none"> • CKGEN_HSE_CLK [40][42][43] • CKGEN_HSI_CLK [40][43] • CKGEN_VHSI_CLK [40][42][43] • CKGEN_SPLL_CLK [40][42][43] • CKGEN_FLASH_CLK [40][42][43] • CKGEN_RTC_CLK [40] • CKGEN_LSI_CLK [40][42][43] • CKGEN_LSI_128K_CLK [40][42][43] • CKGEN_HSE_DIV2_CLK [40][42][43] • CKGEN_VHSI_DIV2_CLK [40][42][43] • CKGEN_HSI_DIV2_CLK [40][43] • CKGEN_SPLL_DIV2_CLK [40][42][43] • CKGEN_BUS_CLK [40][42][43] • CKGEN_SYS_CLK [40][42][43] • CKGEN_ADC_SPLLDIV_CLK [43] • CKGEN_HSE_DIV1_CLK [42][43] • CKGEN_VHSI_DIV1_CLK [42][43] • CKGEN_HSI_DIV1_CLK [43] • CKGEN_SPLL_DIV1_CLK [42][43]
-----------	---------------	---

Returns

void

Definition at line 722 of file AC784xx_Ckgen_Reg.c.

4.3.3.46 Ckgen_Reg_SetClkSrcDiv1()

```
LOCAL_INLINE void Ckgen_Reg_SetClkSrcDiv1 (
    uint32 Value,
    uint32 Mask,
    uint32 Pos )
```

Set clock source div1 division.

Note

Function ID: DES_CKGEN_API_318

Parameters

in	<i>Value</i>	division value to set
in	<i>Mask</i>	register value mask
in	<i>Pos</i>	register position

Returns

void

Definition at line 285 of file AC784xx_Ckgen_Reg.h.

4.3.3.47 Ckgen_Reg_SetClkSrcDiv2()

```
LOCAL_INLINE void Ckgen_Reg_SetClkSrcDiv2 (
    uint32 Value,
    uint32 Mask,
    uint32 Pos )
```

Set clock source div2 division.

Note

Function ID: DES_CKGEN_API_319

Parameters

in	<i>Value</i>	division value to set
in	<i>Mask</i>	register value mask
in	<i>Pos</i>	register position

Returns

void

Definition at line 298 of file AC784xx_Ckgen_Reg.h.

4.3.3.48 Ckgen_Reg_SetCommPeriphClkMux()

```
void Ckgen_Reg_SetCommPeriphClkMux (
    Ckgen_ClkIdType Clk,
    Ckgen_ClkIdType ClkSrc )
```

Set common peripheral clock mux.

Note

Function ID: DES_CKGEN_API_205

Parameters

in	<i>Clk</i>	clock id, value can be one of the list value <ul style="list-style-type: none"> • CKGEN_I2C0_CLK [40][42][43] • CKGEN_I2C1_CLK [42][43] • CKGEN_I2C2_CLK [43] • CKGEN_TIMER_CLK [40][42][43] • CKGEN_SPI0_CLK [40][42][43] • CKGEN_SPI1_CLK [40][42][43] • CKGEN_SPI2_CLK [40][42][43] • CKGEN_SPI3_CLK [42][43] • CKGEN_SPI4_CLK [43] • CKGEN_ADC0_CLK [40][42][43] • CKGEN_ADC1_CLK [40][42][43] • CKGEN_PCT_CLK [40][43] • CKGEN_EIO_CLK [40][42][43] • CKGEN_UART0_CLK [40][42][43] • CKGEN_UART1_CLK [40][42][43] • CKGEN_UART2_CLK [40][42][43] • CKGEN_UART3_CLK [40][42][43] • CKGEN_UART4_CLK [43] • CKGEN_UART5_CLK [43] • CKGEN_UART6_CLK [43] • CKGEN_UART7_CLK [43]
in	<i>ClkSrc</i>	clock id, value can be one of the list value <ul style="list-style-type: none"> • CKGEN_OFF_CLK [40][42][43] • CKGEN_HSE_DIV2_CLK [40][42][43] • CKGEN_HSI_DIV2_CLK [40][42][43] • CKGEN_VHSI_DIV2_CLK [40][42][43] • CKGEN_SPLL_DIV2_CLK [40][42][43] • CKGEN_ADC_SPLLDIV_CLK [43]

Returns

void

Set common peripheral clock mux.

Note

Function ID: DES_CKGEN_API_205

Parameters

in	<i>Clk</i>	<p>clock id, value can be one of the list value</p> <ul style="list-style-type: none"> • CKGEN_I2C0_CLK [40][42][43] • CKGEN_I2C1_CLK [42][43] • CKGEN_I2C2_CLK [43] • CKGEN_TIMER_CLK [40][42][43] • CKGEN_SPI0_CLK [40][42][43] • CKGEN_SPI1_CLK [40][42][43] • CKGEN_SPI2_CLK [40][42][43] • CKGEN_SPI3_CLK [42][43] • CKGEN_SPI4_CLK [43] • CKGEN_ADC0_CLK [40][42][43] • CKGEN_ADC1_CLK [40][42][43] • CKGEN_PCT_CLK [40][43] • CKGEN_EIO_CLK [40][42][43] • CKGEN_UART0_CLK [40][42][43] • CKGEN_UART1_CLK [40][42][43] • CKGEN_UART2_CLK [40][42][43] • CKGEN_UART3_CLK [40][42][43] • CKGEN_UART4_CLK [43] • CKGEN_UART5_CLK [43] • CKGEN_UART6_CLK [43] • CKGEN_UART7_CLK [43]
in	<i>ClkSrc</i>	<p>clock id, value can be one of the list value</p> <ul style="list-style-type: none"> • CKGEN_OFF_CLK [40][42][43] • CKGEN_HSE_DIV2_CLK [40][42][43] • CKGEN_HSI_DIV2_CLK [40][42][43] • CKGEN_VHSI_DIV2_CLK [40][42][43] • CKGEN_SPLL_DIV2_CLK [40][42][43] • CKGEN_ADC_SPLLDIV_CLK [43]

Returns

void

Definition at line 807 of file AC784xx_Ckgen_Reg.c.

4.3.3.49 Ckgen_Reg_SetHSEDIV1ClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetHSEDIV1ClkDiv (
    uint32 Div )
```

Set HSE div1 clock divider.

Note

Function ID: DES_CKGEN_API_345

Parameters

in	<i>Div</i>	division value to set
----	------------	-----------------------

Returns

void

Definition at line 618 of file AC784xx_Ckgen_Reg.h.

4.3.3.50 Ckgen_Reg_SetHSEDIV2ClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetHSEDIV2ClkDiv (
    uint32 Div )
```

Set HSE div2 clock divider.

Note

Function ID: DES_CKGEN_API_347

Parameters

in	<i>Div</i>	division value to set
----	------------	-----------------------

Returns

void

Definition at line 639 of file AC784xx_Ckgen_Reg.h.

4.3.3.51 Ckgen_Reg_SetHSIDIV1ClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetHSIDIV1ClkDiv (
    uint32 Div )
```

Set HSI div1 clock divider.

Note

Function ID: DES_CKGEN_API_353

Parameters

<i>in</i>	<i>Div</i>	division value to set
-----------	------------	-----------------------

Returns

void

Definition at line 706 of file AC784xx_Ckgen_Reg.h.

4.3.3.52 Ckgen_Reg_SetHSIDIV2ClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetHSIDIV2ClkDiv (  
    uint32 Div )
```

Set HSI div2 clock divider.

Note

Function ID: DES_CKGEN_API_355

Parameters

<i>in</i>	<i>Div</i>	division value to set
-----------	------------	-----------------------

Returns

void

Definition at line 735 of file AC784xx_Ckgen_Reg.h.

4.3.3.53 Ckgen_Reg_SetLPMux()

```
LOCAL_INLINE void Ckgen_Reg_SetLPMux (  
    uint32 Val )
```

Set low power clock mux.

Note

Function ID: DES_CKGEN_API_331

Parameters

in	<i>Val</i>	division value to set
----	------------	-----------------------

Returns

void

Definition at line 465 of file AC784xx_Ckgen_Reg.h.

4.3.3.54 Ckgen_Reg_SetPCTClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetPCTClkDiv (  
    uint32 Div )
```

Set PCT clock divider.

Note

Function ID: DES_CKGEN_API_335

Parameters

in	<i>Div</i>	division value to set
----	------------	-----------------------

Returns

void

Definition at line 513 of file AC784xx_Ckgen_Reg.h.

4.3.3.55 Ckgen_Reg_SetPeriphEnable()

```
LOCAL_INLINE void Ckgen_Reg_SetPeriphEnable (  
    uint32 Periph,  
    boolean Enable )
```

Enable/Disbale Periph clock.

Note

Function ID: DES_CKGEN_API_326

Parameters

in	<i>Periph</i>	peripheral id
in	<i>Enable</i>	enable or disable

Returns

void

Definition at line 400 of file AC784xx_Ckgen_Reg.h.

4.3.3.56 Ckgen_Reg_SetPllRefClk()

```
LOCAL_INLINE void Ckgen_Reg_SetPllRefClk (
    uint32 PllRefClk )
```

Set pll reference clock.

Note

Function ID: DES_CKGEN_API_312

Parameters

in	<i>PllRefClk</i>	pll reference clock register value
----	------------------	------------------------------------

Returns

void

Definition at line 206 of file AC784xx_Ckgen_Reg.h.

4.3.3.57 Ckgen_Reg_SetPwmClkMux()

```
void Ckgen_Reg_SetPwmClkMux (
    Ckgen_ClkIdType Clk,
    Ckgen_ClkIdType ClkSrc )
```

Set pwm clock mux.

Note

Function ID: DES_CKGEN_API_204

Parameters

in	<i>Clk</i>	clock id, value can be one of the list value <ul style="list-style-type: none"> • CKGEN_PWM0_CLK [40][42][43] • CKGEN_PWM1_CLK [40][42][43] • CKGEN_PWM2_CLK [40][42][43] • CKGEN_PWM3_CLK [40][42][43] • CKGEN_PWM4_CLK [40][42][43] • CKGEN_PWM5_CLK [40][42][43] • CKGEN_PWM6_CLK [43] • CKGEN_PWM7_CLK [43]
in	<i>ClkSrc</i>	clock id, value can be one of the list value <ul style="list-style-type: none"> • CKGEN_HSE_DIV1_CLK [40][42][43] • CKGEN_HSI_DIV1_CLK [40][42][43] • CKGEN_VHSI_DIV1_CLK [40][42][43] • CKGEN_SPLL_DIV1_CLK [40][42][43] • CKGEN_PWM_EXT_CLK0 [40][42][43] • CKGEN_PWM_EXT_CLK1 [40][42][43] • CKGEN_PWM_EXT_CLK2 [40][42][43]

Returns

void

Definition at line 904 of file AC784xx_Ckgen_Reg.c.

4.3.3.58 Ckgen_Reg_SetRunModeBusClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetRunModeBusClkDiv (
    uint8 Div )
```

Set bus clock division in run mode.

Note

Function ID: DES_CKGEN_API_302

Parameters

in	<i>Div</i>	clock division to set
----	------------	-----------------------

Returns

void

Definition at line 97 of file AC784xx_Ckgen_Reg.h.

4.3.3.59 Ckgen_Reg_SetRunModeSysClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetRunModeSysClkDiv (  
    uint8 Div )
```

Set system clock division in run mode.

Note

Function ID: DES_CKGEN_API_306

Parameters

in	<i>Div</i>	clock division to set
----	------------	-----------------------

Returns

void

Definition at line 140 of file AC784xx_Ckgen_Reg.h.

4.3.3.60 Ckgen_Reg_SetRunModeSysClkSrc()

```
LOCAL_INLINE void Ckgen_Reg_SetRunModeSysClkSrc (  
    uint8 SysClkSrc )
```

Set system clock source in run mode.

Note

Function ID: DES_CKGEN_API_308

Parameters

in	<i>SysClkSrc</i>	clock source to set
----	------------------	---------------------

Returns

void

Definition at line 161 of file AC784xx_Ckgen_Reg.h.

4.3.3.61 Ckgen_Reg_SetSPLLClkMux()

```
void Ckgen_Reg_SetSPLLClkMux (
    Ckgen_ClkIdType ClkSrc )
```

Set spll clock mux.

Note

Function ID: DES_CKGEN_API_209

Parameters

in	ClkSrc	clock source id, value can be one of the list value <ul style="list-style-type: none">CKGEN_HSI_CLK [40][43]CKGEN_VHSI_CLK [42]CKGEN_HSE_CLK [40][42][43]
----	--------	---

Returns

void

Definition at line 668 of file AC784xx_Ckgen_Reg.c.

4.3.3.62 Ckgen_Reg_SetSPLLDIV1ClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetSPLLDIV1ClkDiv (
    uint32 Div )
```

Set SPLl div1 clock divider.

Note

Function ID: DES_CKGEN_API_341

Parameters

in	Div	division value to set
----	-----	-----------------------

Returns

void

Definition at line 576 of file AC784xx_Ckgen_Reg.h.

4.3.3.63 Ckgen_Reg_SetSPLLDIV2ClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetSPLLDIV2ClkDiv (
    uint32 Div )
```

Set SPLL div2 clock divider.

Note

Function ID: DES_CKGEN_API_343

Parameters

in	<i>Div</i>	division value to set
----	------------	-----------------------

Returns

void

Definition at line 597 of file AC784xx_Ckgen_Reg.h.

4.3.3.64 Ckgen_Reg_SetTPIUClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetTPIUClkDiv (
    uint32 Div )
```

Set TPIU clock divider.

Note

Function ID: DES_CKGEN_API_337

Parameters

in	<i>Div</i>	division value to set
----	------------	-----------------------

Returns

void

Definition at line 534 of file AC784xx_Ckgen_Reg.h.

4.3.3.65 Ckgen_Reg_SetVHSIDIV1ClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetVHSIDIV1ClkDiv (
    uint32 Div )
```

Set VHSI div1 clock divider.

Note

Function ID: DES_CKGEN_API_349

Parameters

<i>in</i>	<i>Div</i>	division value to set
-----------	------------	-----------------------

Returns

void

Definition at line 660 of file AC784xx_Ckgen_Reg.h.

4.3.3.66 Ckgen_Reg_SetVHSIDIV2ClkDiv()

```
LOCAL_INLINE void Ckgen_Reg_SetVHSIDIV2ClkDiv (  
    uint32 Div )
```

Set VHSI div2 clock divider.

Note

Function ID: DES_CKGEN_API_351

Parameters

<i>in</i>	<i>Div</i>	division value to set
-----------	------------	-----------------------

Returns

void

Definition at line 681 of file AC784xx_Ckgen_Reg.h.

4.4 Ckgen_Hal.c File Reference

ckgen hal source file.

```
#include "Ckgen_Hal.h"  
#include "Spm_Hal.h"  
#include "AC784xx_Ckgen_Reg.h"  
#include "AC784xx_Spm_Reg.h"
```

Functions

- LOCAL_INLINE uint8 [Ckgen_Hal_GetFlashClkFreq](#) (void)
get flash clock frequency
- LOCAL_INLINE void [Ckgen_Hal_SetFlashClkFreq](#) (uint8 FlashFreq)
set flash clock frequency
- LOCAL_INLINE uint8 [Ckgen_Hal_GetFlashLockStatusReg](#) (void)
get flash lock status
- LOCAL_INLINE Hal_StatusType [Ckgen_Hal_WaitClktoStability](#) (Ckgen_ClkIdType Clk)
Wait for the clock source to stabilize.
- LOCAL_INLINE uint32 [Ckgen_Hal_DivToRegValue](#) (uint32 Div)
Convert division actual value to register value.
- LOCAL_INLINE uint32 [Ckgen_Hal_DivToActualValue](#) (uint32 Div)
Convert division register value to actual value.
- LOCAL_INLINE uint32 [Ckgen_Hal_ClkoutDivToActualValue](#) (uint32 Div)
Convert division register value to actual value.
- LOCAL_INLINE uint32 [Ckgen_Hal_PrevDivToRegValue](#) (uint32 Div)
Convert prevdiv actual value to register value.
- LOCAL_INLINE uint32 [Ckgen_Hal_PosDivToRegValue](#) (uint32 Div)
Convert posdiv actual value to register value.
- LOCAL_INLINE uint32 [Ckgen_Hal_PrevDivToActualVal](#) (uint32 Div)
Convert prevdiv register value to actual value.
- LOCAL_INLINE uint32 [Ckgen_Hal_PosDivToActualVal](#) (uint32 Div)
Convert posdiv register value to actual value.
- Hal_StatusType [Ckgen_Hal_SetPeriphClkDiv](#) (Ckgen_ClkIdType Clk, uint8 Div)
Set peripheral clock division.
- Hal_StatusType [Ckgen_Hal_SetPeriphClkMux](#) (Ckgen_ClkIdType Clk, Ckgen_ClkIdType ClkSrc)
Set peripheral clock mux.
- Ckgen_ClkIdType [Ckgen_Hal_GetClkMux](#) (Ckgen_ClkIdType Clk)
Get clock source.
- Hal_StatusType [Ckgen_Hal_EnablePeriphClk](#) (Ckgen_BusClkIdType Clk, boolean IsEnable)
Enable clock.
- Hal_StatusType [Ckgen_Hal_SetSysClk](#) (const [Ckgen_SysClkCfgType](#) *CfgPtr)
Set sysclk.
- Hal_StatusType [Ckgen_Hal_GetFreq](#) (Ckgen_ClkIdType Clk, uint32 *Freq)
Get clock frequency.
- Hal_StatusType [Ckgen_Hal_GetClkStatus](#) (Ckgen_ClkIdType Clk)
Get clock status.
- Hal_StatusType [Ckgen_Hal_DistributeClk](#) (const [Ckgen_ClkDistributeCfgType](#) *CfgPtr)
Wait clock to Stable and distribute system and module clock.
- Hal_StatusType [Ckgen_Hal_InitClk](#) (const [Ckgen_ClkTreeCfgType](#) *CfgPtr)
Initialize clocks source.

4.4.1 Detailed Description

ckgen hal source file.

4.4.2 Function Documentation

4.4.2.1 Ckgen_Hal_ClkoutDivToActualValue()

```
LOCAL_INLINE uint32 Ckgen_Hal_ClkoutDivToActualValue (
    uint32 Div )
```

Convert division register value to actual value.

Note

Function ID: DES_CKGEN_API_138

Parameters

in	<i>Div</i>	Division register value
----	------------	-------------------------

Returns

uint32: Division actual value

Definition at line 430 of file Ckgen_Hal.c.

4.4.2.2 Ckgen_Hal_DistributeClk()

```
Hal_StatusType Ckgen_Hal_DistributeClk (
    const Ckgen_ClkDistributeCfgType * CfgPtr )
```

Wait clock to Stable and distribute system and module clock.

Note

Function ID: DES_CKGEN_API_002

Parameters

in	<i>CfgPtr</i>	the pointer to the Ckgen_ClkDistributeCfgType structure
----	---------------	---

Returns

Hal_StatusType: Distribute success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 2222 of file Ckgen_Hal.c.

4.4.2.3 Ckgen_Hal_DivToActualValue()

```
LOCAL_INLINE uint32 Ckgen_Hal_DivToActualValue (
    uint32 Div )
```

Convert division register value to actual value.

Note

Function ID: DES_CKGEN_API_139

Parameters

<i>in</i>	<i>Div</i>	Division register value
-----------	------------	-------------------------

Returns

uint32: Division actual value

Definition at line 418 of file Ckgen_Hal.c.

4.4.2.4 Ckgen_Hal_DivToRegValue()

```
LOCAL_INLINE uint32 Ckgen_Hal_DivToRegValue (  
    uint32 Div )
```

Convert division actual value to register value.

Note

Function ID: DES_CKGEN_API_140

Parameters

<i>in</i>	<i>Div</i>	Division actual value
-----------	------------	-----------------------

Returns

uint32: Division register value

Definition at line 406 of file Ckgen_Hal.c.

4.4.2.5 Ckgen_Hal_EnablePeriphClk()

```
Hal_StatusType Ckgen_Hal_EnablePeriphClk (  
    Ckgen_BusClkIdType Clk,  
    boolean IsEnable )
```

Enable clock.

Enable or disbale bus clock.

Note

Function ID: DES_CKGEN_API_004

Parameters

in	<i>Clk</i>	clock id
in	<i>IsEnable</i>	turn the clock on or off

Returns

Hal_StatusType: Operation success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 1127 of file Ckgen_Hal.c.

4.4.2.6 Ckgen_Hal_GetClkMux()

```
Ckgen_ClkIdType Ckgen_Hal_GetClkMux (
    Ckgen_ClkIdType Clk )
```

Get clock source.

Get the clock source of the clock.

Note

Function ID: DES_CKGEN_API_007

Parameters

in	<i>Clk</i>	clock id
----	------------	----------

Returns

Ckgen_ClkIdType: clock source

Definition at line 1098 of file Ckgen_Hal.c.

4.4.2.7 Ckgen_Hal_GetClkStatus()

```
Hal_StatusType Ckgen_Hal_GetClkStatus (
    Ckgen_ClkIdType Clk )
```

Get clock status.

Note

Function ID: DES_CKGEN_API_009

Parameters

<i>in</i>	<i>Clk</i>	clock id, the range is bus clock clkout and hse hsi vhsi spll
-----------	------------	---

Returns

Hal_StatusType: clock status range is the STATUS_CLK_ON STATUS_CLK_OFF STATUS_CLK_STABLE STATUS_CLK_UNSTABLE

Definition at line 1955 of file Ckgen_Hal.c.

4.4.2.8 Ckgen_Hal_GetFlashClkFreq()

```
LOCAL_INLINE uint8 Ckgen_Hal_GetFlashClkFreq (
    void )
```

get flash clock frequency

Note

Function ID: DES_CKGEN_API_150

Returns

uint32: flash clock frequency

Definition at line 67 of file Ckgen_Hal.c.

4.4.2.9 Ckgen_Hal_GetFlashLockStatusReg()

```
LOCAL_INLINE uint8 Ckgen_Hal_GetFlashLockStatusReg (
    void )
```

get flash lock status

Note

Function ID: DES_CKGEN_API_148

Returns

uint32: lock status

Definition at line 134 of file Ckgen_Hal.c.

4.4.2.10 Ckgen_Hal_GetFreq()

```
Hal_StatusType Ckgen_Hal_GetFreq (
    Ckgen_ClkIdType Clk,
    uint32 * Freq )
```

Get clock frequency.

Note

Function ID: DES_CKGEN_API_005

Parameters

in	<i>Clk</i>	clock id
in	<i>Freq</i>	the pointer to the uint32 value

Returns

Hal_StatusType: Get success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 1874 of file Ckgen_Hal.c.

4.4.2.11 Ckgen_Hal_InitClk()

```
Hal_StatusType Ckgen_Hal_InitClk (  
    const Ckgen_ClkTreeCfgType * CfgPtr )
```

Initialize clocks source.

Note

Function ID: DES_CKGEN_API_001

Parameters

in	<i>CfgPtr</i>	the pointer to the Ckgen_AllClkCfgType structure
----	---------------	--

Returns

Hal_StatusType: Distribute success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 2277 of file Ckgen_Hal.c.

4.4.2.12 Ckgen_Hal_PosDivToActualVal()

```
LOCAL_INLINE uint32 Ckgen_Hal_PosDivToActualVal (  
    uint32 Div )
```

Convert posdiv register value to actual value.

Note

Function ID: DES_CKGEN_API_134

Parameters

in	<i>Div</i>	Division register value
----	------------	-------------------------

Returns

uint32: Division actual value

Definition at line 514 of file Ckgen_Hal.c.

4.4.2.13 Ckgen_Hal_PosDivToRegValue()

```
LOCAL_INLINE uint32 Ckgen_Hal_PosDivToRegValue (
    uint32 Div )
```

Convert posdiv actual value to register value.

Note

Function ID: DES_CKGEN_API_136

Parameters

in	<i>Div</i>	Division actual value
----	------------	-----------------------

Returns

uint32: Division register value

Definition at line 474 of file Ckgen_Hal.c.

4.4.2.14 Ckgen_Hal_PreDivToActualVal()

```
LOCAL_INLINE uint32 Ckgen_Hal_PreDivToActualVal (
    uint32 Div )
```

Convert prediv register value to actual value.

Note

Function ID: DES_CKGEN_API_135

Parameters

in	<i>Div</i>	Division register value
----	------------	-------------------------

Returns

uint32: Division actual value

Definition at line 491 of file Ckgen_Hal.c.

4.4.2.15 Ckgen_Hal_PreDivToRegValue()

```
LOCAL_INLINE uint32 Ckgen_Hal_PreDivToRegValue (
    uint32 Div )
```

Convert prediv actual value to register value.

Note

Function ID: DES_CKGEN_API_137

Parameters

in	<i>Div</i>	Division actual value
----	------------	-----------------------

Returns

uint32: Division register value

Definition at line 452 of file Ckgen_Hal.c.

4.4.2.16 Ckgen_Hal_SetFlashClkFreq()

```
LOCAL_INLINE void Ckgen_Hal_SetFlashClkFreq (
    uint8 FlashFreq )
```

set flash clock frequency

Note

Function ID: DES_CKGEN_API_149

Parameters

in	<i>FlashFreq</i>	flash clock frequency
----	------------------	-----------------------

Returns

void

Definition at line 78 of file Ckgen_Hal.c.

4.4.2.17 Ckgen_Hal_SetPeriphClkDiv()

```
Hal_StatusType Ckgen_Hal_SetPeriphClkDiv (
    Ckgen_ClkIdType Clk,
    uint8 Div )
```

Set peripheral clock division.

Note

Function ID: DES_CKGEN_API_006

Parameters

<i>in</i>	<i>Clk</i>	clock id,value can be one of the list value <ul style="list-style-type: none">• CKGEN_CAN0_CLK [40][42][43]• CKGEN_CAN1_CLK [40][42][43]• CKGEN_CAN2_CLK [40][42][43]• CKGEN_CAN3_CLK [40][42][43]• CKGEN_CAN4_CLK [42][43]• CKGEN_CAN5_CLK [42][43]• CKGEN_CAN0_TS_CLK [40][42]• CKGEN_CAN1_TS_CLK [40][42]• CKGEN_CAN2_TS_CLK [40][42]• CKGEN_CAN3_TS_CLK [40][42]• CKGEN_CAN4_TS_CLK [40][42]• CKGEN_CAN5_TS_CLK [40][42]• CKGEN_PCT_CLK [40][42][43]• CKGEN_TPIU_CLK [40][42][43]
<i>in</i>	<i>Div</i>	clock division

Returns

Hal_StatusType: Set success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 546 of file Ckgen_Hal.c.

4.4.2.18 Ckgen_Hal_SetPeriphClkMux()

```
Hal_StatusType Ckgen_Hal_SetPeriphClkMux (
    Ckgen_ClkIdType Clk,
    Ckgen_ClkIdType ClkSrc )
```

Set peripheral clock mux.

Set the peripheral clock of the source.

Note

Function ID: DES_CKGEN_API_008

Parameters

in	<i>Clk</i>	clock id
in	<i>ClkSrc</i>	clock source

Returns

Hal_StatusType: Operation success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 944 of file Ckgen_Hal.c.

4.4.2.19 Ckgen_Hal_SetSysClk()

```
Hal_StatusType Ckgen_Hal_SetSysClk (
    const Ckgen_SysClkCfgType * CfgPtr )
```

Set sysclk.

Note

Function ID: DES_CKGEN_API_003

Parameters

in	<i>CfgPtr</i>	The pointer to the Ckgen_SysClkCfgType structure
----	---------------	--

Returns

Hal_StatusType: Set success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 1845 of file Ckgen_Hal.c.

4.4.2.20 Ckgen_Hal_WaitClktoStability()

```
LOCAL_INLINE Hal_StatusType Ckgen_Hal_WaitClktoStability (
    Ckgen_ClkIdType Clk )
```

Wait for the clock soure to stabilize.

Note

Function ID: DES_CKGEN_API_142

Parameters

in	<i>Clk</i>	clock id, the rang is vhsi hsi hse spll
----	------------	---

Returns

Hal_StatusType: whether clock is stable, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 318 of file Ckgen_Hal.c.

4.5 Ckgen_Hal.h File Reference

Ckgen hal interface for SDK.

```
#include "Device_Register.h"
```

Classes

- struct [Ckgen_ClkMuxCfgType](#)
peripheral clock mux configure structure.
- struct [Ckgen_ClkDivCfgType](#)
peripheral clock division configure structure.
- struct [Ckgen_ClkoutCfgType](#)
clkout clock configure structure.
- struct [Ckgen_LPCLkCfgType](#)
low power clock configure structure.
- struct [Ckgen_ExternalClkFreqCfgType](#)
external clock frequency configure structure.
- struct [Ckgen_PLICfgType](#)
PLL clock configure structure.
- struct [Ckgen_ClkSrcCfgType](#)
clock source configure structure.
- struct [Ckgen_XoscClkCfgType](#)
Xosc clock configure structure.
- struct [Ckgen_SysClkCfgType](#)
system clock configure structure.
- struct [Ckgen_ClkDistributeCfgType](#)
Distribute clock configure structure.
- struct [Ckgen_ClkTreeCfgType](#)
Clock tree configure structure.

Functions

- Hal_StatusType [Ckgen_Hal_GetClkStatus](#) (Ckgen_ClkIdType Clk)
Get clock status.
- Hal_StatusType [Ckgen_Hal_SetPeriphClkMux](#) (Ckgen_ClkIdType Clk, Ckgen_ClkIdType ClkSrc)
Set the peripheral clock of the source.
- Ckgen_ClkIdType [Ckgen_Hal_GetClkMux](#) (Ckgen_ClkIdType Clk)
Get the clock source of the clock.
- Hal_StatusType [Ckgen_Hal_SetPeriphClkDiv](#) (Ckgen_ClkIdType Clk, uint8 Div)
Set peripheral clock division.
- Hal_StatusType [Ckgen_Hal_GetFreq](#) (Ckgen_ClkIdType Clk, uint32 *Freq)
Get clock frequency.
- Hal_StatusType [Ckgen_Hal_EnablePeriphClk](#) (Ckgen_BusClkIdType Clk, boolean IsEnable)

Enable or disable bus clock.

- Hal_StatusType [Ckgen_Hal_SetSysClk](#) (const [Ckgen_SysClkCfgType](#) *CfgPtr)

Set sysclk.

- Hal_StatusType [Ckgen_Hal_DistributeClk](#) (const [Ckgen_ClkDistributeCfgType](#) *CfgPtr)

Wait clock to Stable and distribute system and module clock.

- Hal_StatusType [Ckgen_Hal_InitClk](#) (const [Ckgen_ClkTreeCfgType](#) *CfgPtr)

Initialize clocks source.

4.5.1 Detailed Description

Ckgen hal interface for SDK.

4.5.2 Function Documentation

4.5.2.1 Ckgen_Hal_DistributeClk()

```
Hal_StatusType Ckgen_Hal_DistributeClk (
    const Ckgen\_ClkDistributeCfgType * CfgPtr )
```

Wait clock to Stable and distribute system and module clock.

Note

Function ID: DES_CKGEN_API_002

Parameters

in	<i>CfgPtr</i>	the pointer to the Ckgen_ClkDistributeCfgType structure
----	---------------	---

Returns

Hal_StatusType: Distribute success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 2222 of file Ckgen_Hal.c.

4.5.2.2 Ckgen_Hal_EnablePeriphClk()

```
Hal_StatusType Ckgen_Hal_EnablePeriphClk (
    Ckgen_BusClkIdType Clk,
    boolean IsEnable )
```

Enable or disable bus clock.

Note

Function ID: DES_CKGEN_API_004

Parameters

in	<i>Clk</i>	clock id bus clock ranges are listed below:
in	<i>IsEnable</i>	turn the clock on or off

Returns

Hal_StatusType: Operation success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Enable or disbale bus clock.

Note

Function ID: DES_CKGEN_API_004

Parameters

in	<i>Clk</i>	clock id
in	<i>IsEnable</i>	turn the clock on or off

Returns

Hal_StatusType: Operation success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 1127 of file Ckgen_Hal.c.

4.5.2.3 Ckgen_Hal_GetClkMux()

```
Ckgen_ClkIdType Ckgen_Hal_GetClkMux (  
    Ckgen_ClkIdType Clk )
```

Get the clock source of the clock.

Note

Function ID: DES_CKGEN_API_007

Parameters

in	<i>Clk</i>	clock id, the value ranges are listed below:
----	------------	--

Returns

Ckgen_ClkIdType: clock source id

Get the clock source of the clock.

Note

Function ID: DES_CKGEN_API_007

Parameters

<i>in</i>	<i>Clk</i>	clock id
-----------	------------	----------

Returns

Ckgen_ClkIdType: clock source

Definition at line 1098 of file Ckgen_Hal.c.

4.5.2.4 Ckgen_Hal_GetClkStatus()

```
Hal_StatusType Ckgen_Hal_GetClkStatus (
    Ckgen_ClkIdType Clk )
```

Get clock status.

Note

Function ID: DES_CKGEN_API_009

Parameters

<i>in</i>	<i>Clk</i>	clock id, the value ranges are listed below: <ul style="list-style-type: none">• CKGEN_VHSI_CLK• CKGEN_HSI_CLK• CKGEN_HSI_VLPS_CLK• CKGEN_SPLL_CLK• CKGEN_HSE_CLK
-----------	------------	---

Returns

Hal_StatusType: clock status range is the STATUS_CLK_ON STATUS_CLK_OFF STATUS_CLK_STABLE STATUS_CLK_UNSTABLE

Note

Function ID: DES_CKGEN_API_009

Parameters

<i>in</i>	<i>Clk</i>	clock id, the range is bus clock clkout and hse hsi vhsi spll
-----------	------------	---

Returns

Hal_StatusType: clock status range is the STATUS_CLK_ON STATUS_CLK_OFF STATUS_CLK_STABLE STATUS_CLK_UNSTABLE

Definition at line 1955 of file Ckgen_Hal.c.

4.5.2.5 Ckgen_Hal_GetFreq()

```
Hal_StatusType Ckgen_Hal_GetFreq (
    Ckgen_ClkIdType Clk,
    uint32 * Freq )
```

Get clock frequency.

Note

Function ID: DES_CKGEN_API_005

Parameters

in	Clk	clock id, the value ranges are listed below:
out	Freq	the pointer to the uint32 value

Returns

Hal_StatusType: Get success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Note

Function ID: DES_CKGEN_API_005

Parameters

in	Clk	clock id
in	Freq	the pointer to the uint32 value

Returns

Hal_StatusType: Get success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 1874 of file Ckgen_Hal.c.

4.5.2.6 Ckgen_Hal_InitClk()

```
Hal_StatusType Ckgen_Hal_InitClk (
    const Ckgen_ClkTreeCfgType * CfgPtr )
```

Initialize clocks source.

Note

Function ID: DES_CKGEN_API_001

Parameters

in	<i>CfgPtr</i>	the pointer to the Ckgen_AllClkCfgType structure
----	---------------	--

Returns

Hal_StatusType: Distribute success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 2277 of file Ckgen_Hal.c.

4.5.2.7 Ckgen_Hal_SetPeriphClkDiv()

```
Hal_StatusType Ckgen_Hal_SetPeriphClkDiv (
    Ckgen_ClkIdType Clk,
    uint8 Div )
```

Set peripheral clock division.

Note

Function ID: DES_CKGEN_API_006

Parameters

in	<i>Clk</i>	clock id,value can be one of the list value <ul style="list-style-type: none">• CKGEN_CAN0_CLK [40][42][43]• CKGEN_CAN1_CLK [40][42][43]• CKGEN_CAN2_CLK [40][42][43]• CKGEN_CAN3_CLK [40][42][43]• CKGEN_CAN4_CLK [42][43]• CKGEN_CAN5_CLK [42][43]• CKGEN_CAN0_TS_CLK [40][42]• CKGEN_CAN1_TS_CLK [40][42]• CKGEN_CAN2_TS_CLK [40][42]• CKGEN_CAN3_TS_CLK [40][42]• CKGEN_CAN4_TS_CLK [40][42]• CKGEN_CAN5_TS_CLK [40][42]• CKGEN_PCT_CLK [40][42][43]• CKGEN_TPIU_CLK [40][42][43]
in	<i>Div</i>	clock division

Returns

Hal_StatusType: Set success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 546 of file Ckgen_Hal.c.

4.5.2.8 Ckgen_Hal_SetPeriphClkMux()

```
Hal_StatusType Ckgen_Hal_SetPeriphClkMux (
    Ckgen_ClkIdType Clk,
    Ckgen_ClkIdType ClkSrc )
```

Set the peripheral clock of the source.

Note

Function ID: DES_CKGEN_API_008

Parameters

in	<i>Clk</i>	clock id
in	<i>ClkSrc</i>	clock source

Returns

Hal_StatusType: Set success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Set the peripheral clock of the source.

Note

Function ID: DES_CKGEN_API_008

Parameters

in	<i>Clk</i>	clock id
in	<i>ClkSrc</i>	clock source

Returns

Hal_StatusType: Operation success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 944 of file Ckgen_Hal.c.

4.5.2.9 Ckgen_Hal_SetSysClk()

```
Hal_StatusType Ckgen_Hal_SetSysClk (
    const Ckgen_SysClkCfgType * CfgPtr )
```

Set sysclk.

Note

Function ID: DES_CKGEN_API_003

Parameters

in	<i>CfgPtr</i>	The pointer to the Ckgen_SysClkCfgType structure
----	---------------	--

Returns

Hal_StatusType: Set success or not, the range is the STATUS_SUCCESS STATUS_ERROR

Definition at line 1845 of file Ckgen_Hal.c.

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